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INT CL⁴ G06F

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(54) Manufacture of integrated circuits

(57) An integrated circuit design is constructed from a library of standard cells, at least some of which are available in different sizes having different input requirements, output capabilities and response times. Details of a proposed integrated circuit design are entered into a computer which stores the properties of the standard cells. The computer selects among the the standard cells required in the proposed design for compatible sizes of the cells providing the smallest circuit or the fastest circuit. The computer can also check race conditions in the circuit and that input and output criteria are satisfied. When a satisfactory design has been reached its details are produced as an output which is used to produce layout diagrams from which the integrated circuit is manufactured.

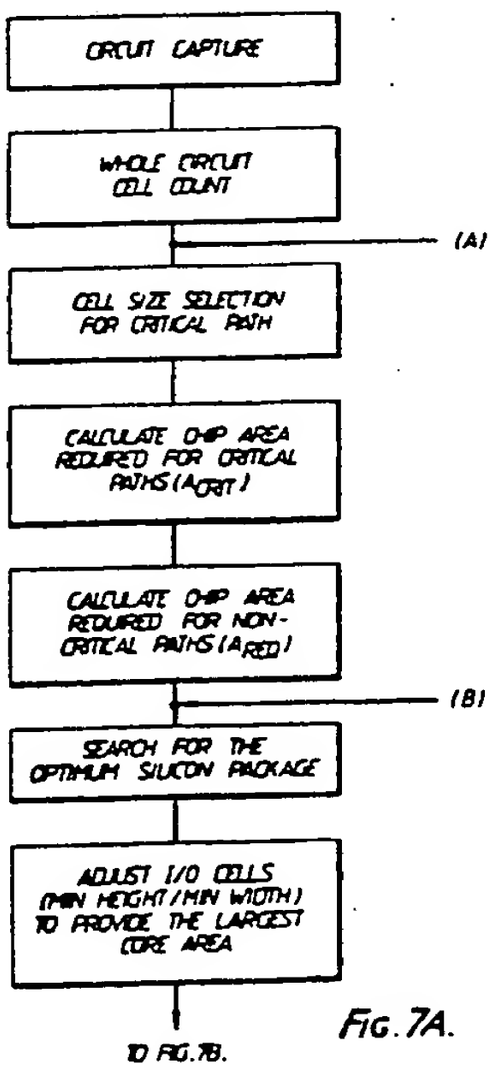

Fig. 7A.

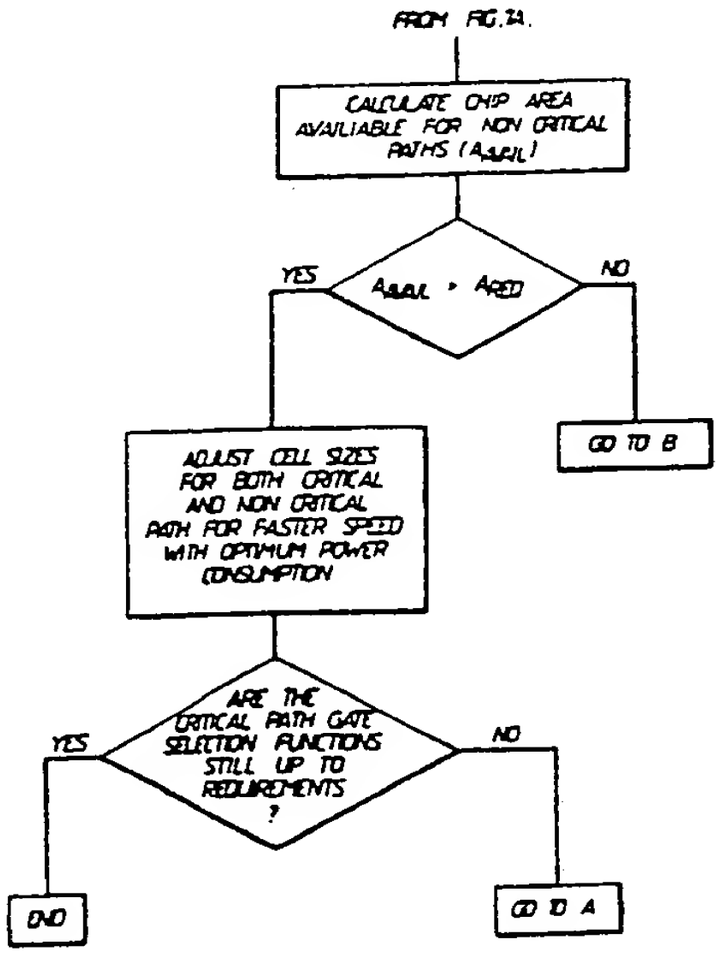

Fig. 7B.

At least one drawing originally filed was informal and the print reproduced here is taken from a later filed formal copy

The claims were filed later than the filing date within the period prescribed by Rule 25(1) of the Patents Rules 1982.

This print takes account of replacement documents submitted after the date of filing to enable the application to comply with the formal requirements of the Patents Rules 1982.

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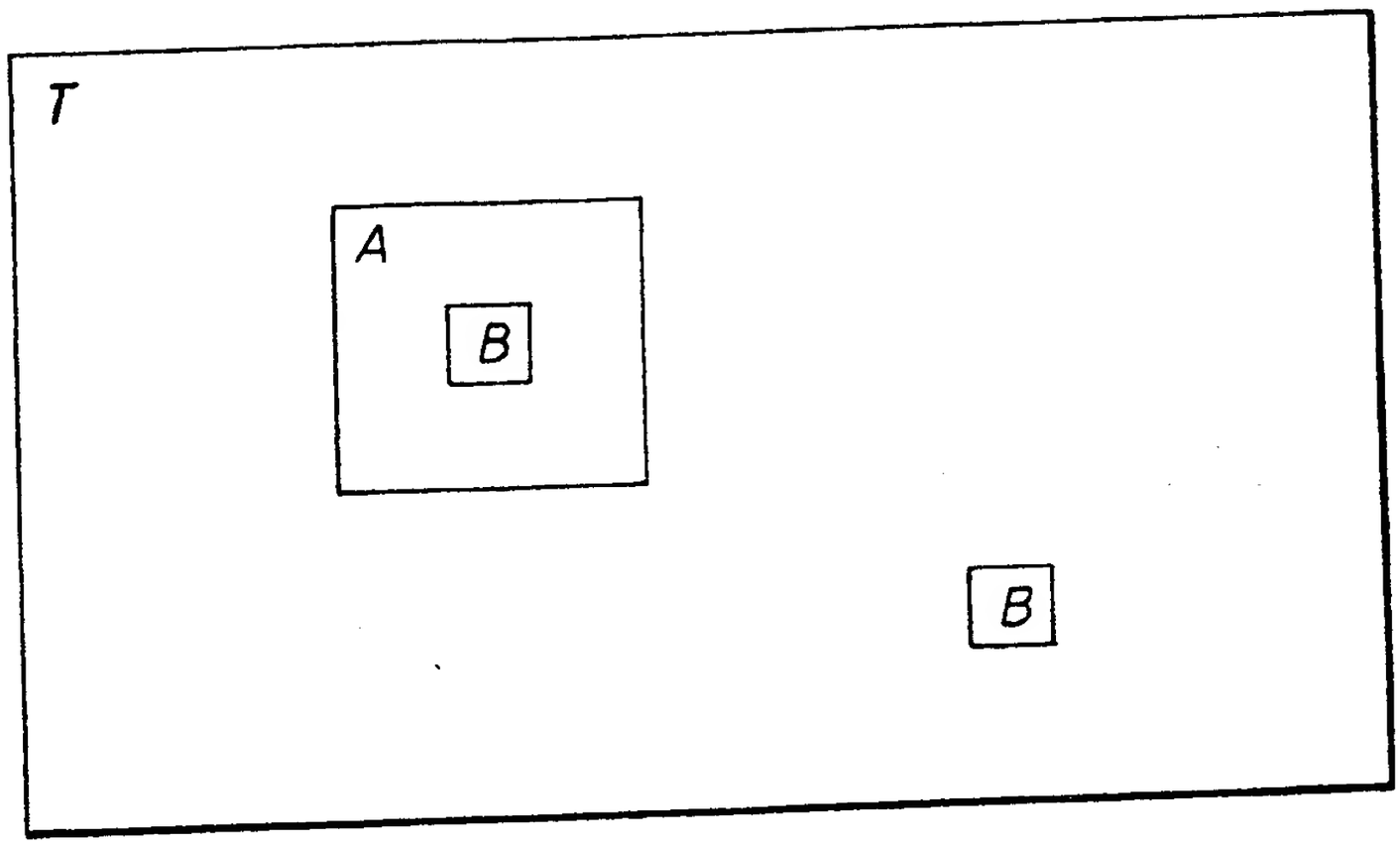

FIG. 1.

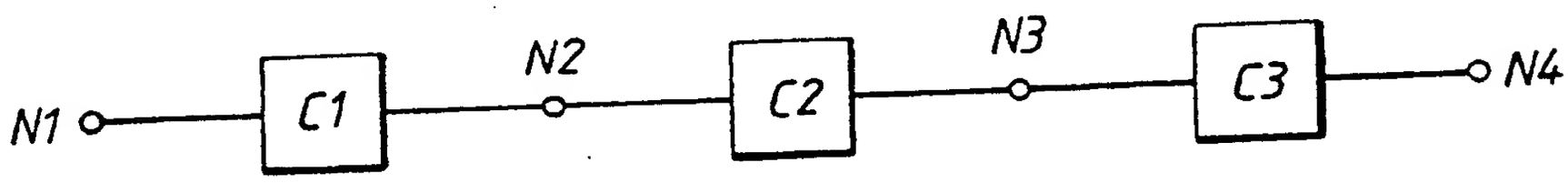

FIG. 2.

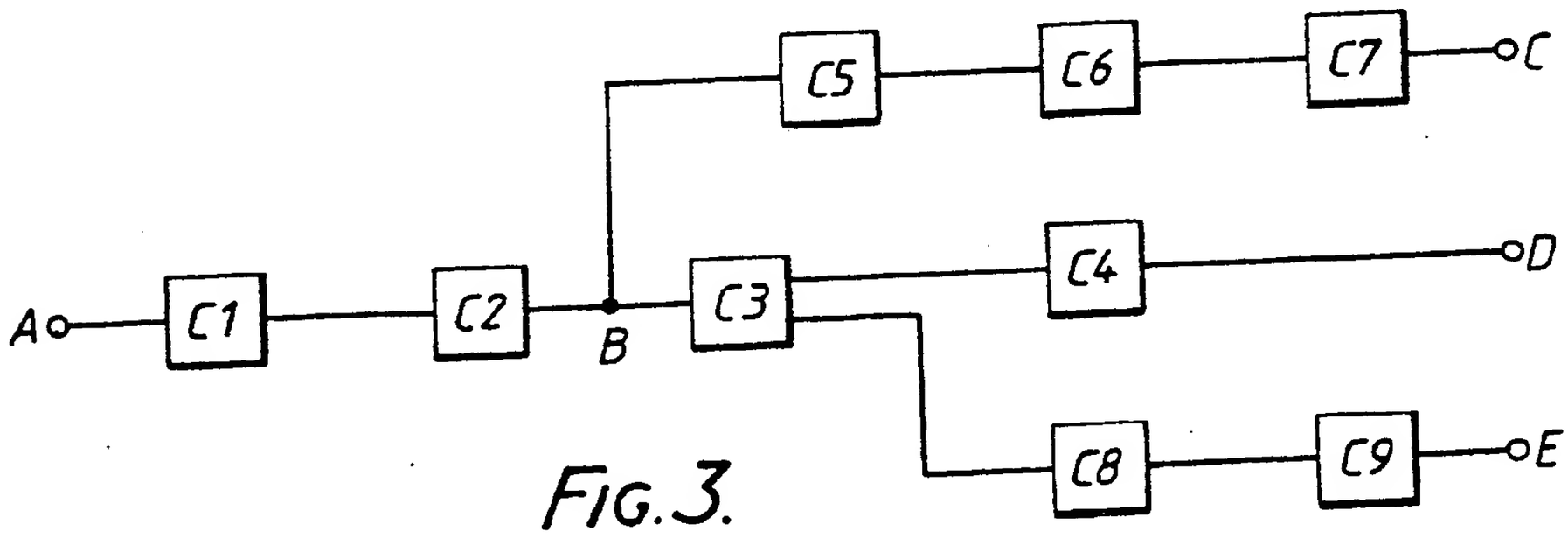

FIG. 3.

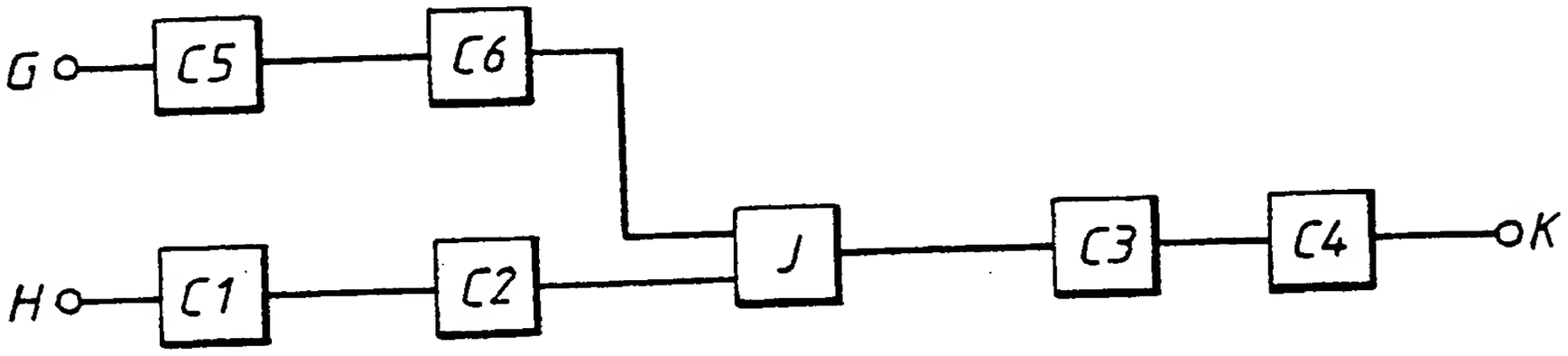

FIG.4.

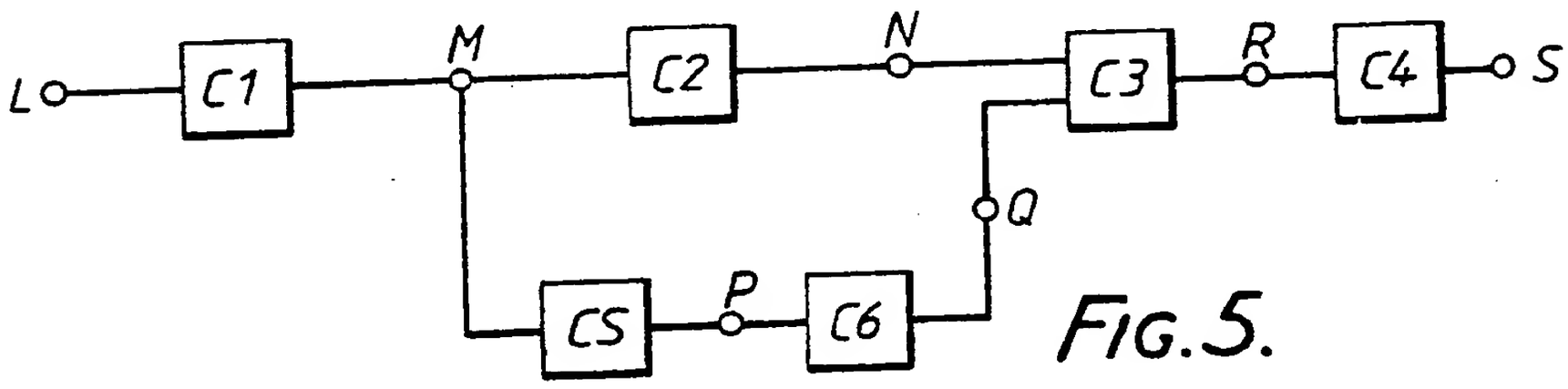

FIG.5.

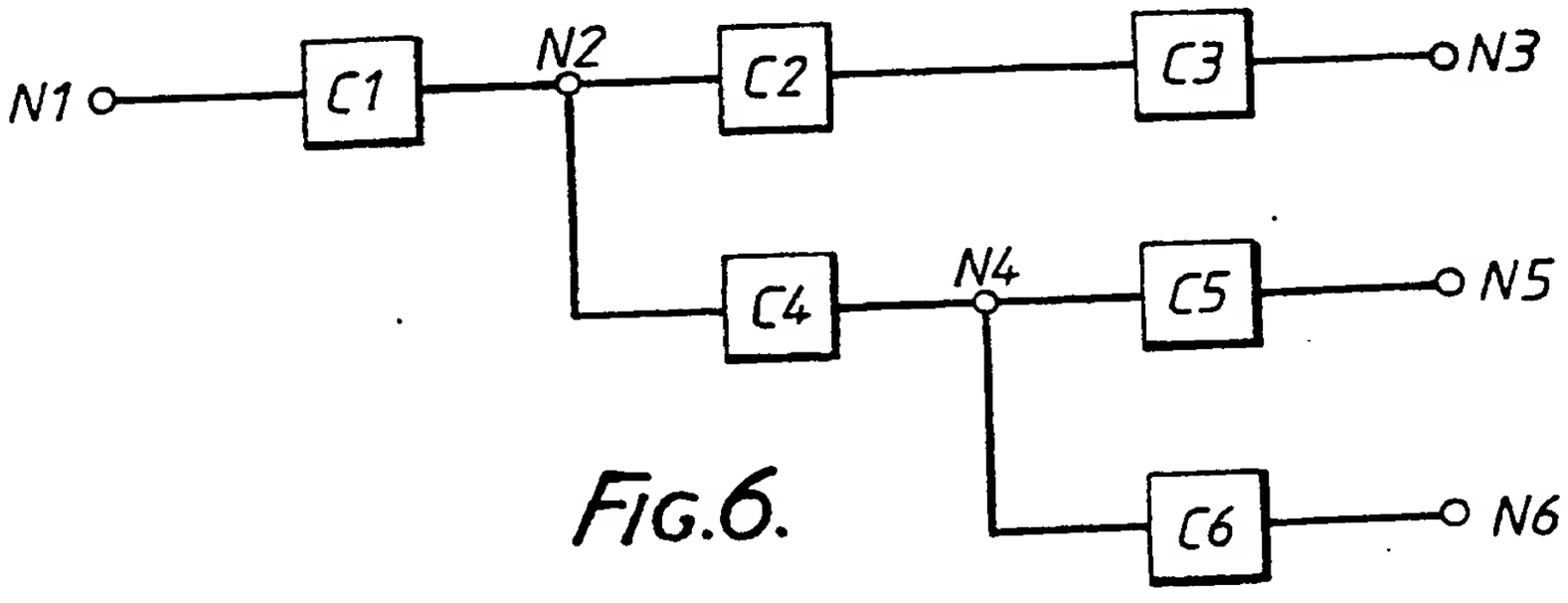

FIG.6.

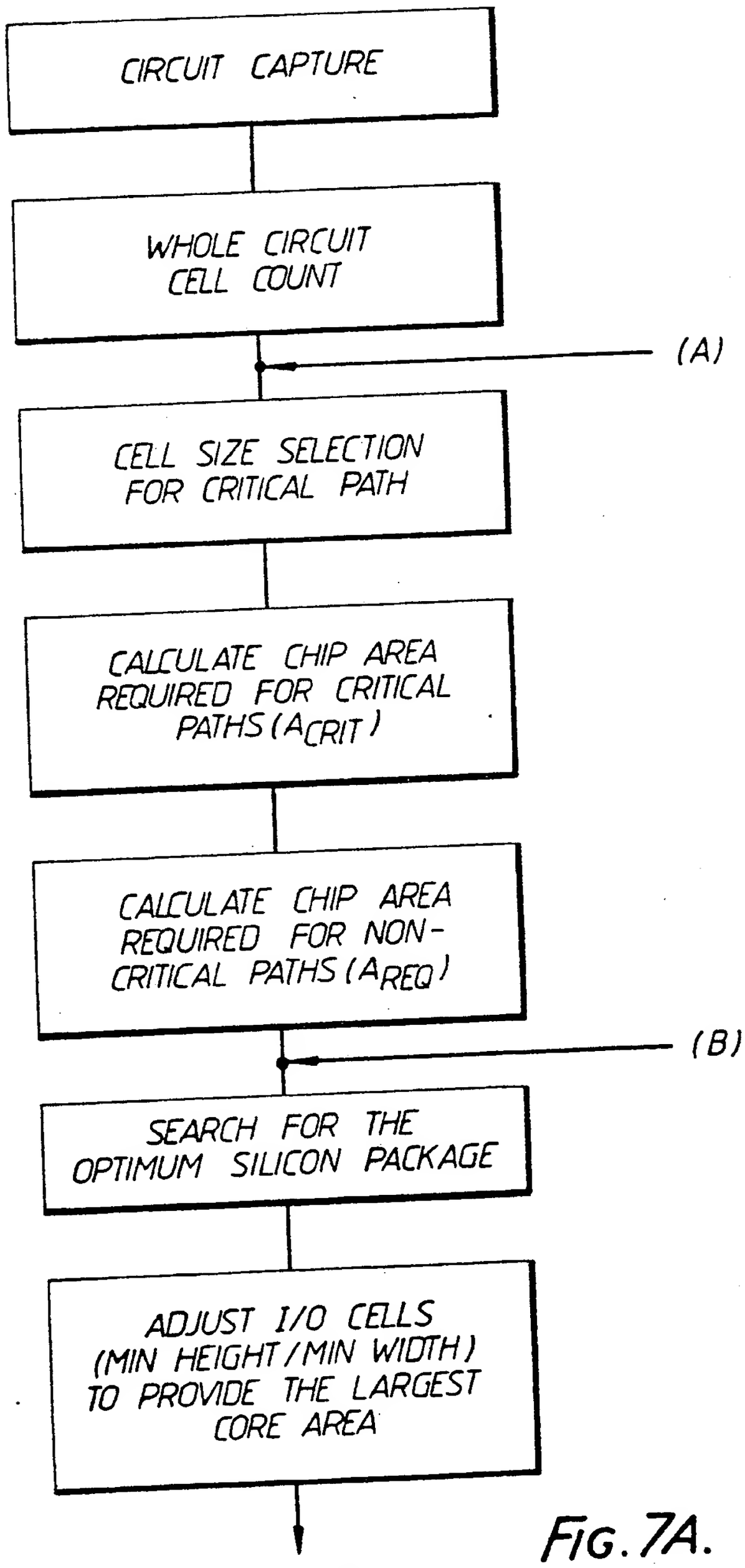
CIRCUIT CAPTURE
WHOLE CIRCUIT CELL COUNT
(A)
CELL SIZE SELECTION FOR CRITICAL PATH
CALCULATE CHIP AREA REQUIRED FOR CRITICAL PATHS (A_{CRIT})
CALCULATE CHIP AREA REQUIRED FOR NON-CRITICAL PATHS (A_{REQ})
(B)
SEARCH FOR THE OPTIMUM SILICON PACKAGE
ADJUST I/O CELLS (MIN HEIGHT/MIN WIDTH) TO PROVIDE THE LARGEST CORE AREA
TO FIG.7B.

FIG. 7A.

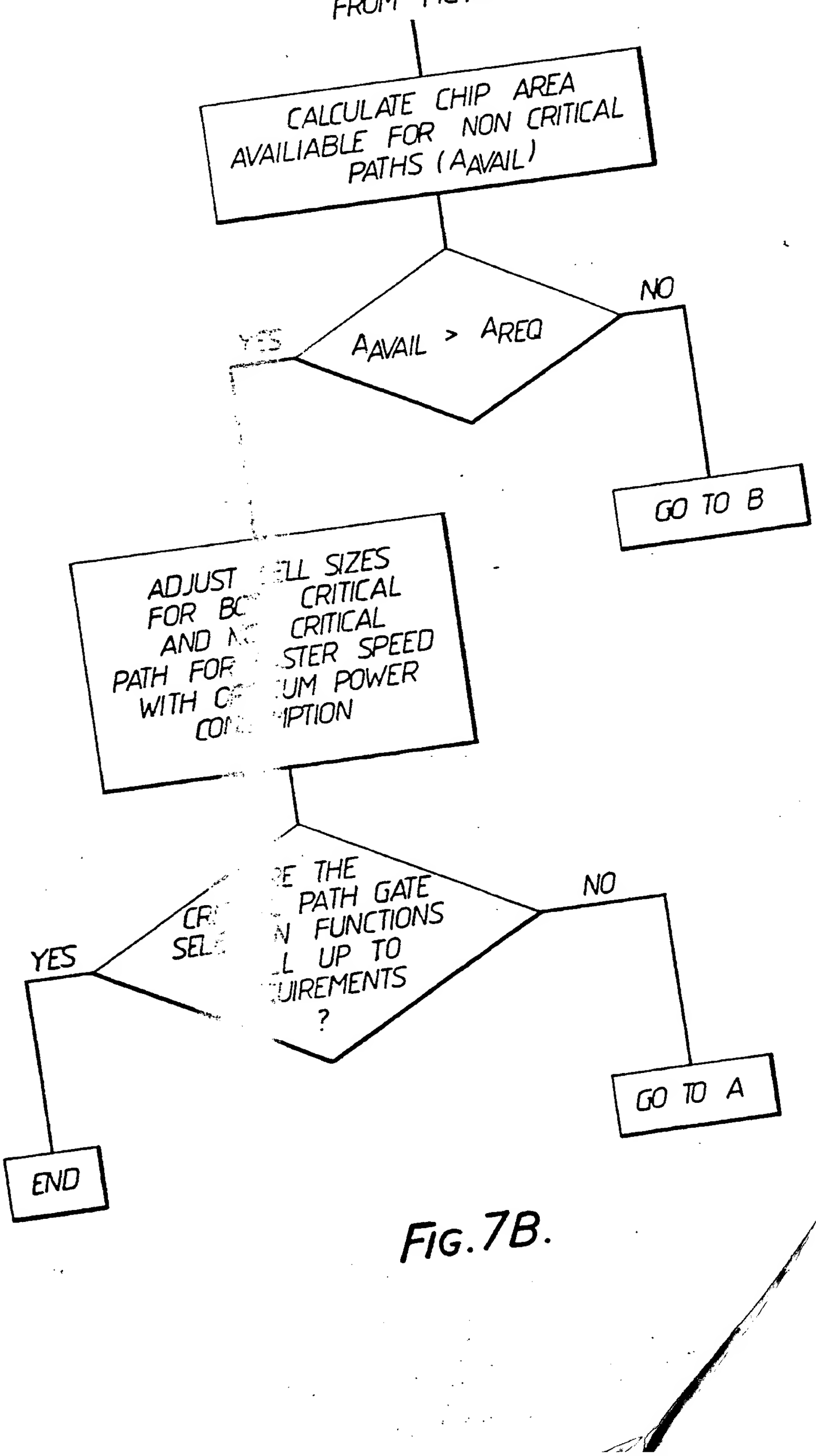
FROM FIG.7A.
CALCULATE CHIP AREA AVAILIABLE FOR NON CRITICAL PATHS (AAVAIL)
AAVAIL > AREQ
NO
YES
GO TO B
ADJUST
FOR BC
AND N
PATH FOR
WITH C
CO
LL SIZES
CRITICAL
CRITICAL
STER SPEED
UM POWER
IPTION
E THE
PATH GATE
N FUNCTIONS
L UP TO
UIREMENTS
?
NO
CR
SEL
YES
GO TO A
END

FIG.7B.

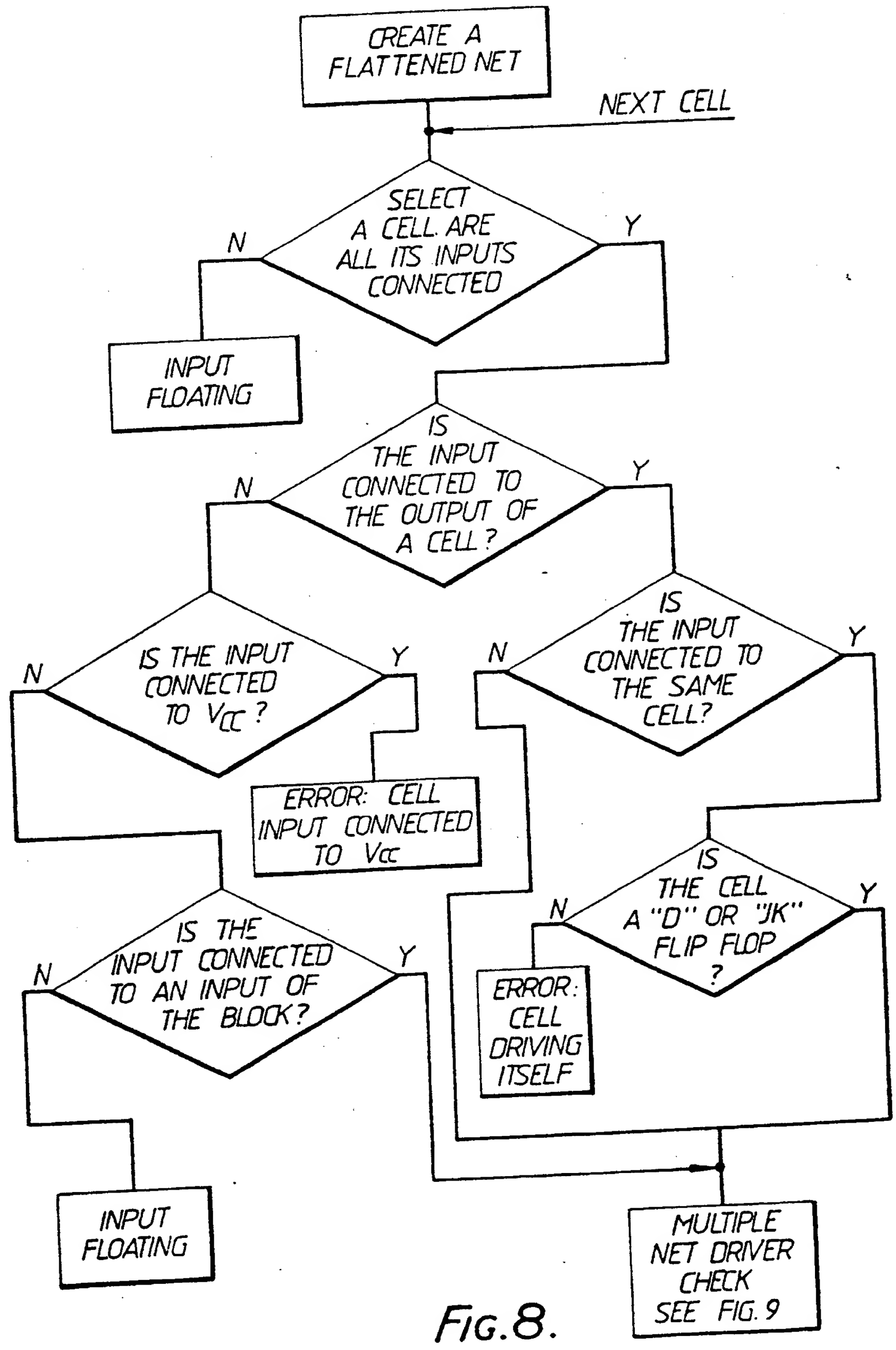
CREATE A FLATTENED NET
NEXT CELL
SELECT A CELL. ARE ALL ITS INPUTS CONNECTED
N
Y
INPUT FLOATING
IS THE INPUT CONNECTED TO THE OUTPUT OF A CELL?
N
Y
IS THE INPUT CONNECTED TO V_{CC} ?
N
Y
ERROR: CELL INPUT CONNECTED TO Vcc
IS THE INPUT CONNECTED TO THE SAME CELL?
N
Y
IS THE CELL A "D" OR "JK" FLIP FLOP ?
N
Y
ERROR: CELL DRIVING ITSELF
IS THE INPUT CONNECTED TO AN INPUT OF THE BLOCK?
N
Y
INPUT FLOATING
MULTIPLE NET DRIVER CHECK SEE FIG. 9

FIG. 8.

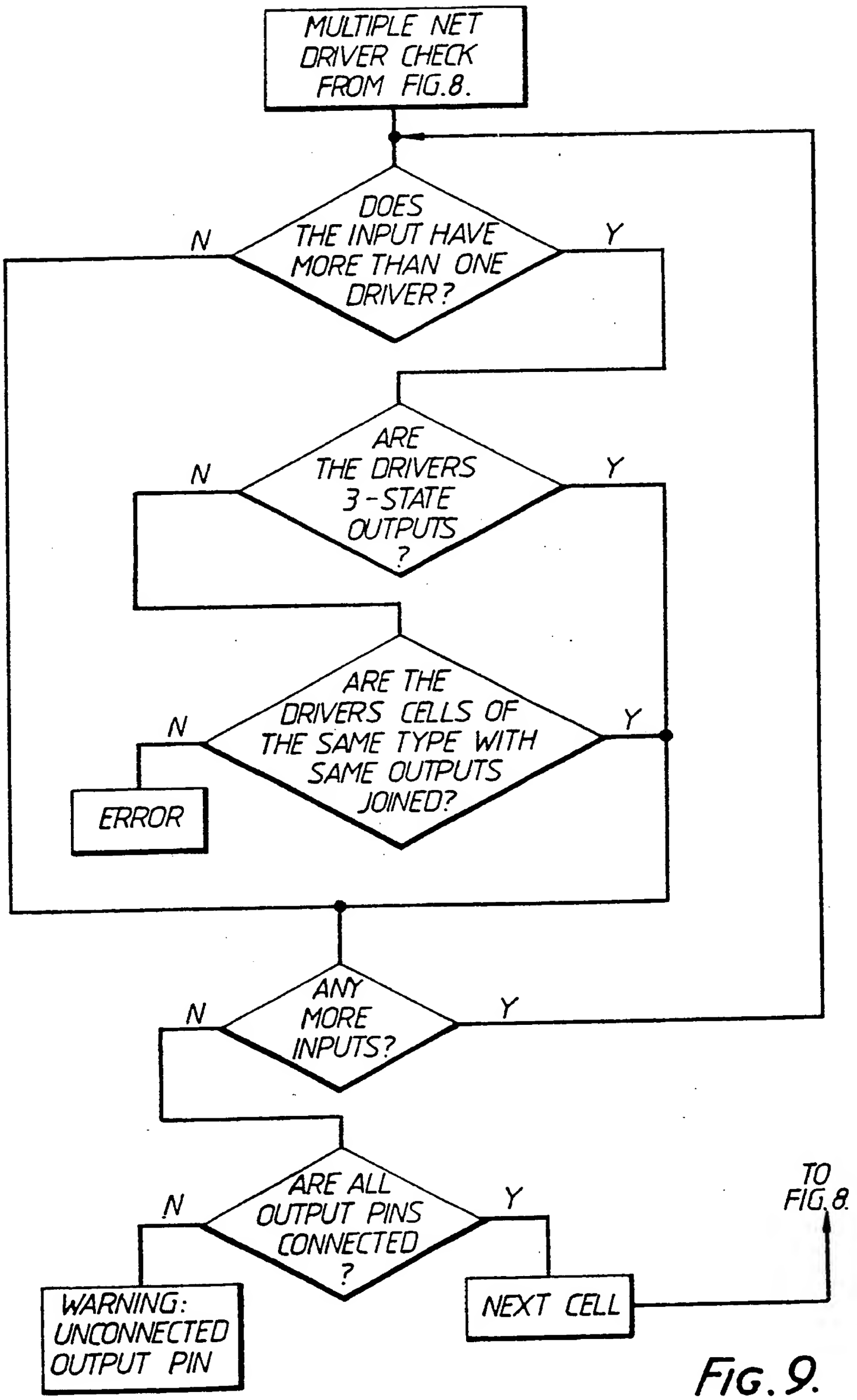
MULTIPLE NET DRIVER CHECK FROM FIG.8.
DOES THE INPUT HAVE MORE THAN ONE DRIVER?
N
Y
ARE THE DRIVERS 3-STATE OUTPUTS ?
N
Y
ARE THE DRIVERS CELLS OF THE SAME TYPE WITH SAME OUTPUTS JOINED?
N
Y
ERROR
ANY MORE INPUTS?
N
Y
ARE ALL OUTPUT PINS CONNECTED ?
N
Y
WARNING: UNCONNECTED OUTPUT PIN
NEXT CELL
TO FIG.8.

FIG. 9.

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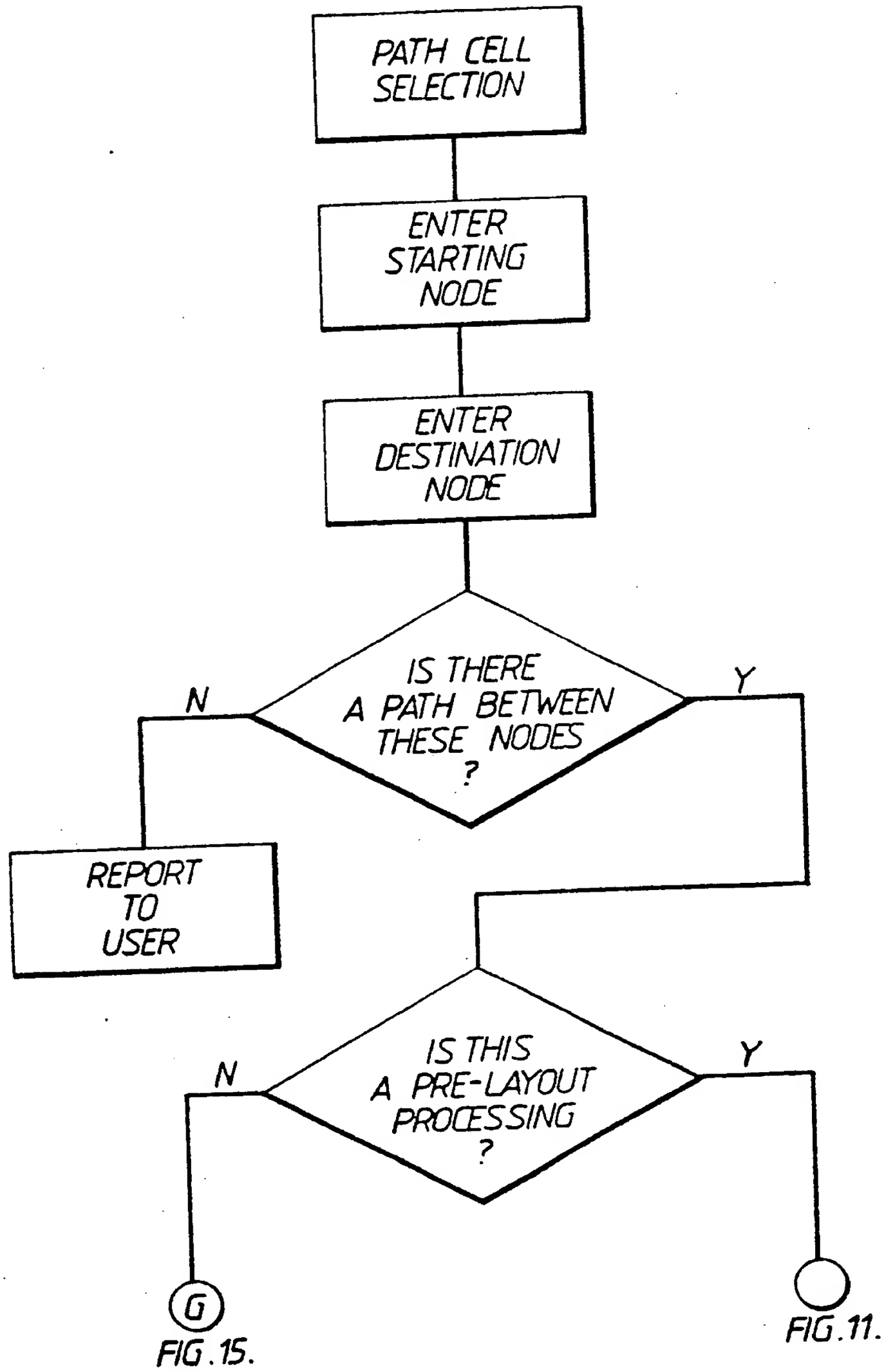
PATH CELL SELECTION
ENTER STARTING NODE
ENTER DESTINATION NODE
IS THERE A PATH BETWEEN THESE NODES ?
N
Y
REPORT TO USER
IS THIS A PRE-LAYOUT PROCESSING ?
N
Y
G
FIG. 15.
FIG. 11.

FIG. 10.

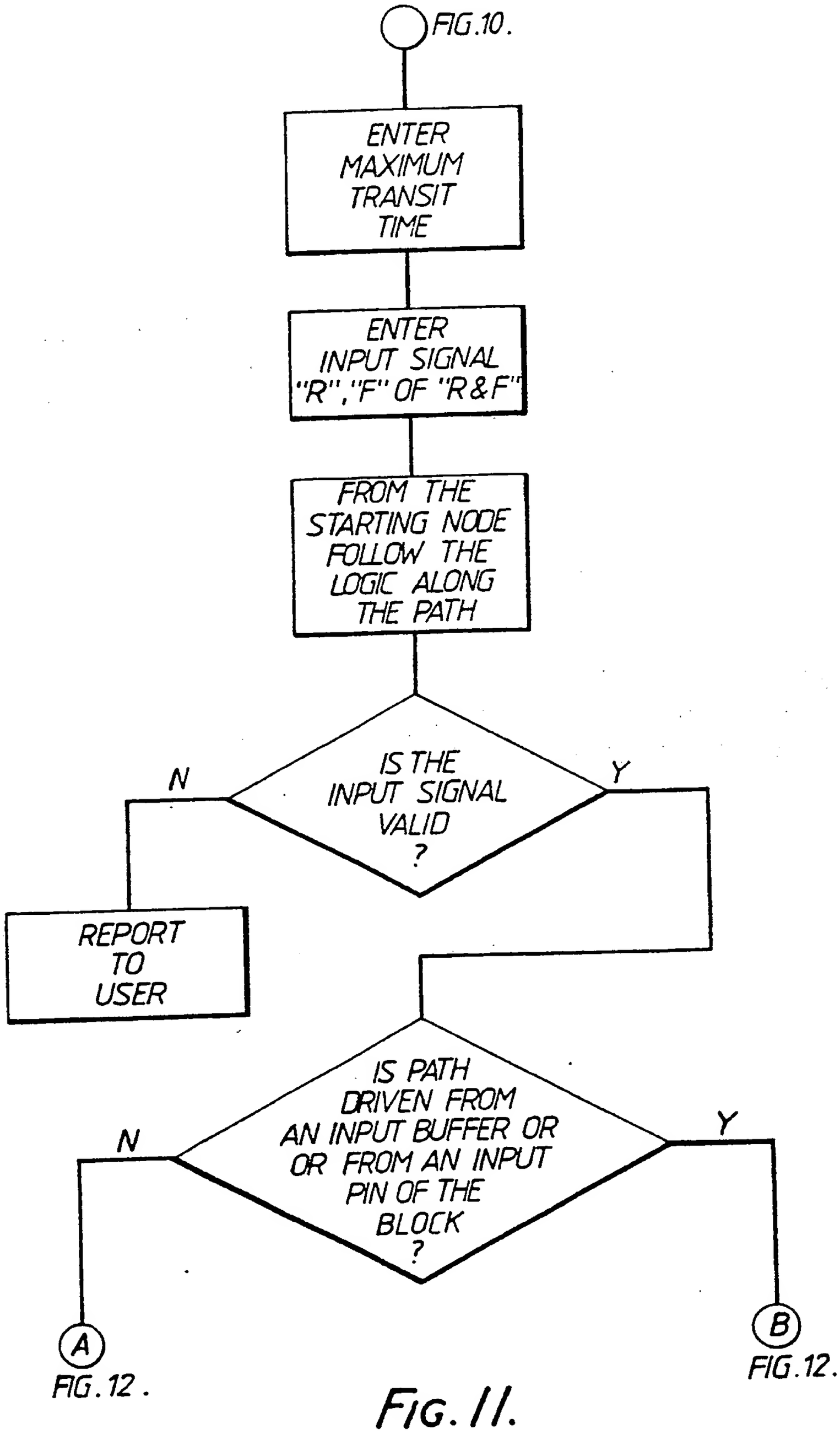
FIG.10.
ENTER MAXIMUM TRANSIT TIME
ENTER INPUT SIGNAL "R","F" OF "R&F"
FROM THE STARTING NODE FOLLOW THE LOGIC ALONG THE PATH
IS THE INPUT SIGNAL VALID ?
N
Y
REPORT TO USER
IS PATH DRIVEN FROM AN INPUT BUFFER OR OR FROM AN INPUT PIN OF THE BLOCK ?
N
Y
A
FIG.12.
B
FIG.12.

FIG. 11.

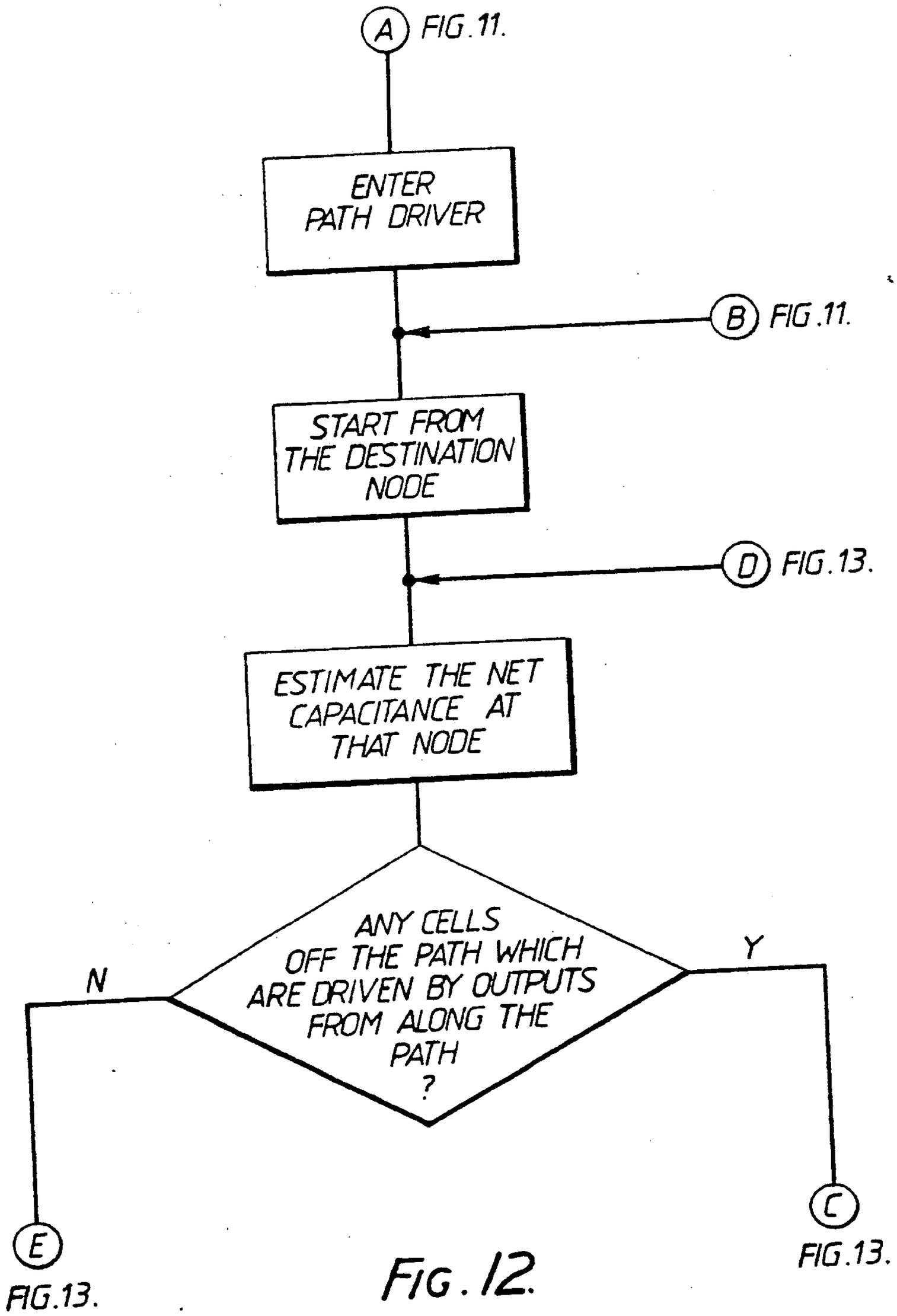
A FIG.11.
ENTER PATH DRIVER
B FIG.11.
START FROM THE DESTINATION NODE
D FIG.13.
ESTIMATE THE NET CAPACITANCE AT THAT NODE
ANY CELLS OFF THE PATH WHICH ARE DRIVEN BY OUTPUTS FROM ALONG THE PATH ?
N
Y
E FIG.13.
C FIG.13.

FIG. 12.

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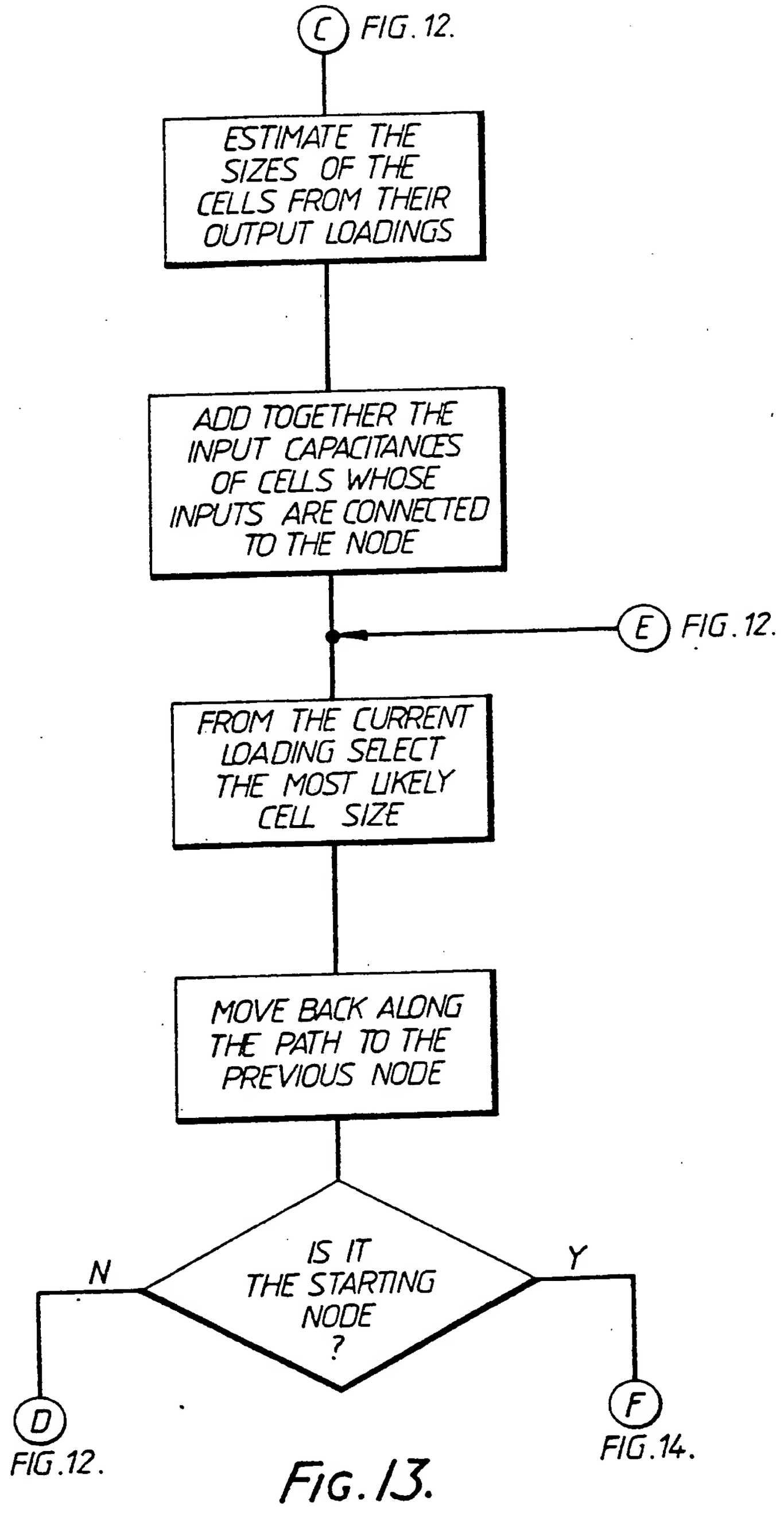


FIG. 13.

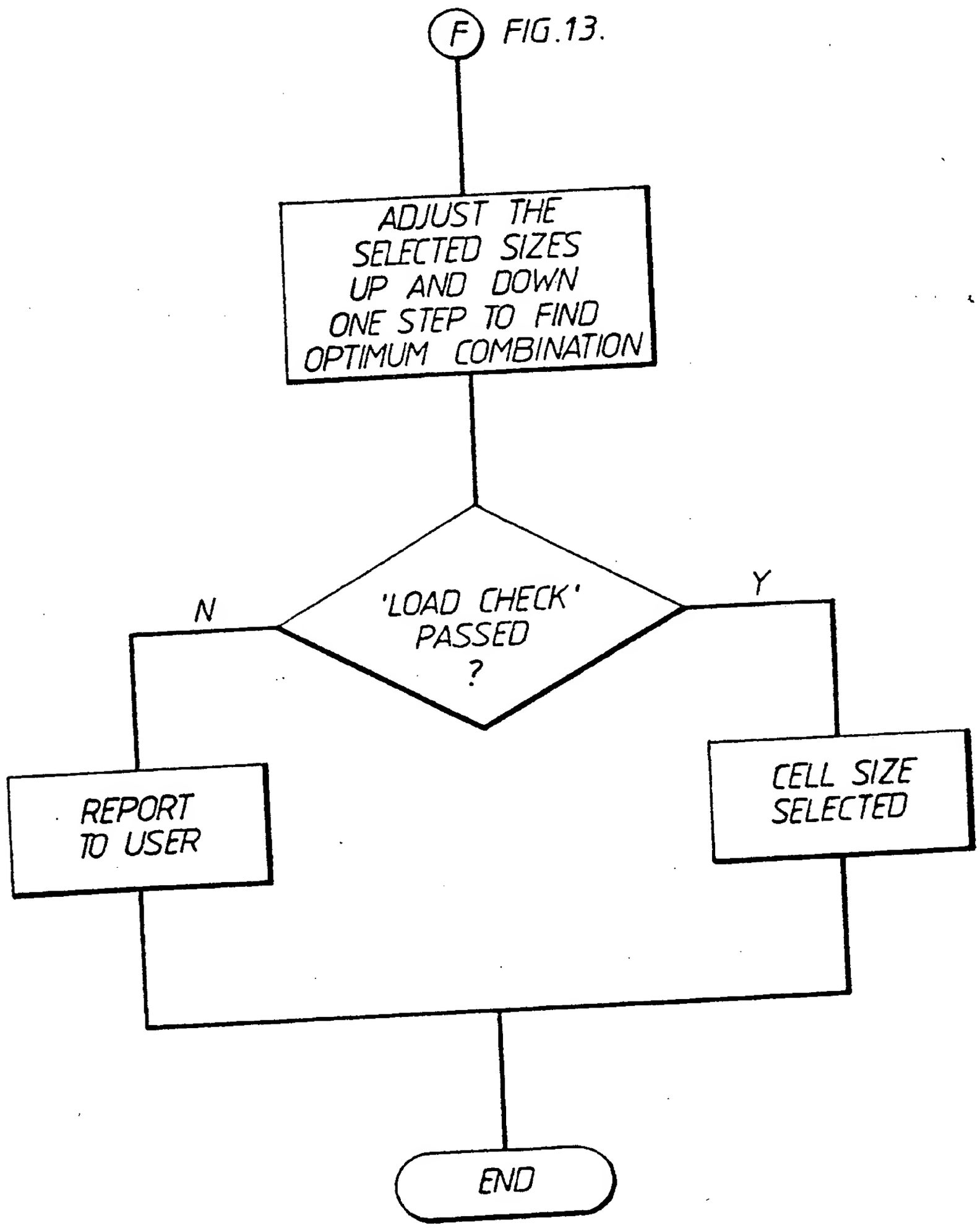

F
ADJUST THE SELECTED SIZES UP AND DOWN ONE STEP TO FIND OPTIMUM COMBINATION
'LOAD CHECK' PASSED ?
N
Y
REPORT TO USER
CELL SIZE SELECTED
END

FIG.13.

FIG.14.

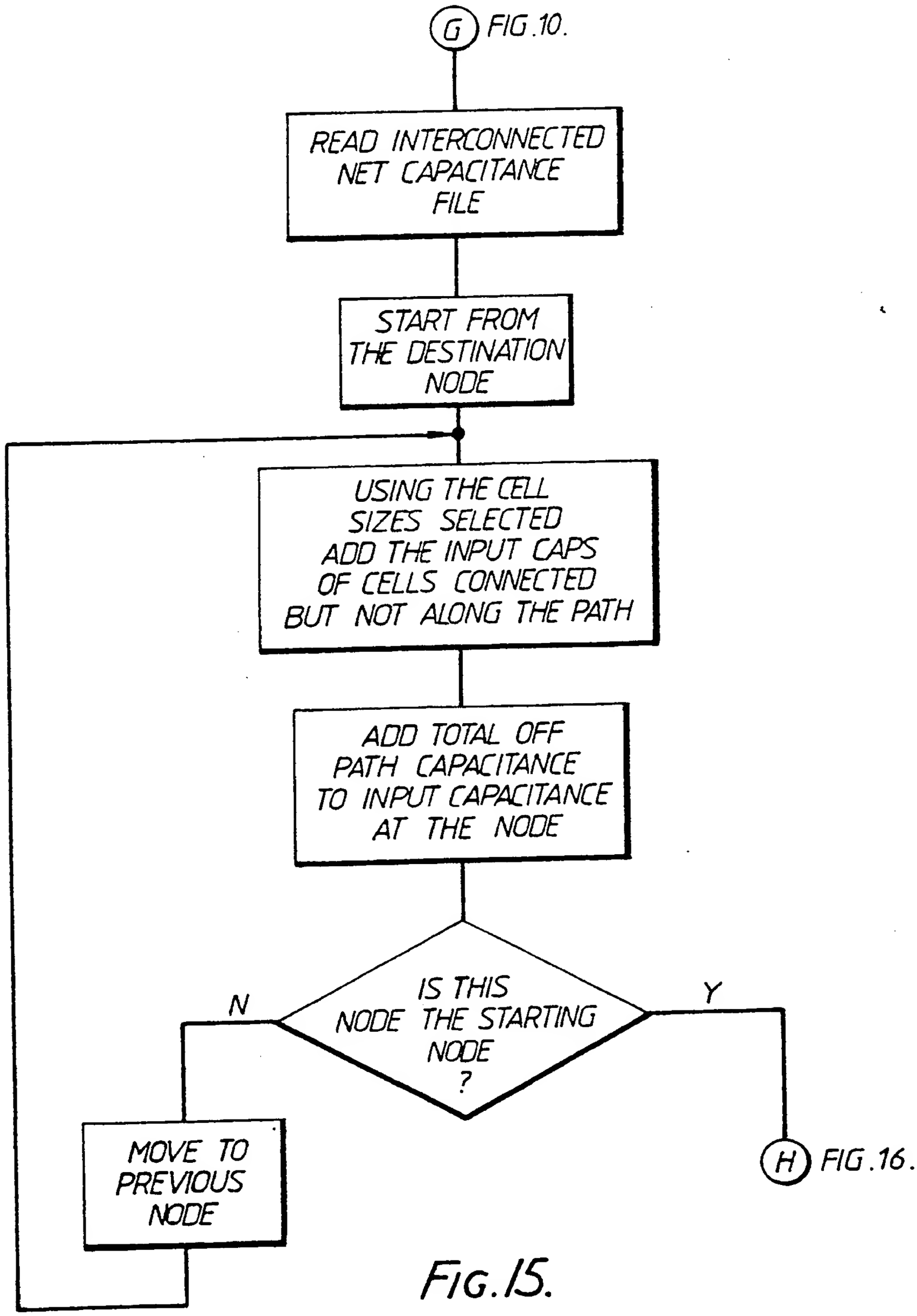

G
FIG.10.
READ INTERCONNECTED NET CAPACITANCE FILE
START FROM THE DESTINATION NODE
USING THE CELL SIZES SELECTED ADD THE INPUT CAPS OF CELLS CONNECTED BUT NOT ALONG THE PATH
ADD TOTAL OFF PATH CAPACITANCE TO INPUT CAPACITANCE AT THE NODE
IS THIS NODE THE STARTING NODE ?
N
Y
MOVE TO PREVIOUS NODE
H
FIG.16.

FIG. 15.

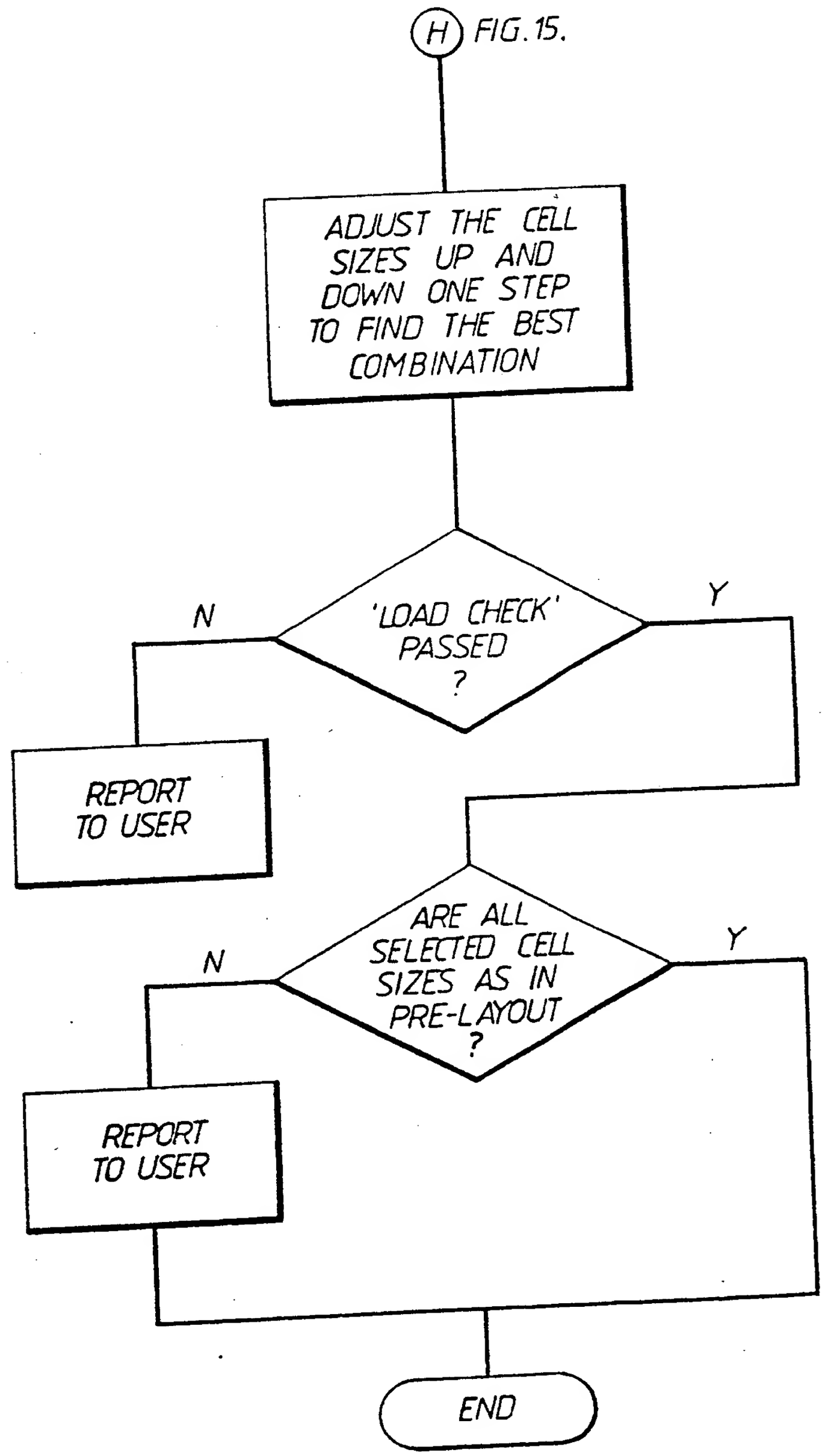

H
ADJUST THE CELL SIZES UP AND DOWN ONE STEP TO FIND THE BEST COMBINATION
'LOAD CHECK' PASSED ?
N
Y
REPORT TO USER
ARE ALL SELECTED CELL SIZES AS IN PRE-LAYOUT ?
N
Y
REPORT TO USER
END

FIG. 15.

FIG. 16.

IMPROVEMENTS RELATING TO THE MANUFACTURE OF INTEGRATED CIRCUITS

This invention relates to the manufacture of integrated circuits and in particular to the design of such circuits using standard units or cells.

Integrated circuits enable complex electronic systems to be constructed at low cost because each integrated circuit includes a large number of components which are fabricated simultaneously using the same series of processes. A difficulty encountered in the use of integrated circuits arises when the particular electronic system to be made requires one or more special types of integrated circuit having different combinations of functional capabilities from those provided by the standard types. This difficulty has been met by manufacturers providing such special types of integrated circuit using so-called standard cells inter-connected as required to produce the particular special combinations of functions. The use of standard cells in this way means that the detailed design of the components within each cell has already been done, and the designer of the special integrated circuit has the relatively simpler job of selecting the standard cells and planning the layout and interconnection of the selected cells to perform the required functions.

It is nonetheless a difficult task for the designer to select the optimum cells to produce the circuit required with the specified performance taking into consideration the loadings imposed by the inputs of cells on the outputs of other cells, the driving abilities of the other cells, the signal propagation delays, the cell response times and the input signal requirements of certain cells. He also needs to bear in mind the amount of semiconductor material required to accommodate the circuit and reduce it to a minimum.

It is an object of the present invention to provide the designer of special integrated circuits with assistance in performing his job.

According to one aspect of the present invention there is provided a method of manufacturing an integrated circuit including entering into a computer in response to a functional specification inputs representing a circuit design containing only selected items from a set of standard units, which design performs the logical functions of the specification, causing the components to derive from a memory recording details of the standard units of the set the response times, input loadings and output drive capabilities of different sizes of the standard units used in the circuit design, causing the computer to determine from the circuit design and the input loadings and the output drive capabilities of standard units when interconnected in accordance with the circuit design selected sizes for the standard units to match in each case the output drive capability of a unit to the total input loading of the unit or units which the particular unit is required to drive, causing the computer to produce an output display of the selected sizes of the standard units used in circuit design, producing from the display layout diagrams of an integrated circuit of the ciruit design using the selected sizes of standard units and using the layout diagrams to fabricate the integrated circuit.

The selection of the sizes of the standard units may be arranged to meet propagation delay specifications for signals along paths in the circuit indicated as being critical. When such critical path specifications have been met the sizes of other standard units may be selected according to one or other of the following criteria:

a. to give the smallest propagation delay time.

b. to require the smallest area of semiconductor material (such as silicon or gallium arsenide) for the construction of the standard units to meet specified timing requirements.

The computer may also be programmed to calculate the signal propagation delay along a selected path for given sizes of standard units, thereby providing an indication of the likely performance of the final integrated circuit.

In addition, the input loadings and output capabilities of the final integrated circuit may be checked against specified values by the computer.

The computer may be running a conventional integrated circuit design program of the kind used in an industry standard computer aided design work station for integrated circuit work, and the invention may utilise features of that program to assist the designer. Examples of such work stations are the Apollo DN300, DN660, DN200, and DN590 series.

The program may be arranged to select the sizes of standard cells to achieve different results in the final integrated circuit. Examples of such different results are as follows:-

1. Fastest signal path. In this case, for the combination of standard cells forming a particular signal path, the program calculates the total signal delay along the path taking into consideration the response times of the different compatible sizes of the standard cells themselves and the delays imposed by the interconnections and input capacitances of the cells, and automatically selects the sizes of cells which provide the fastest signal propagation along the path. The total area of the semiconductor chip required to construct the path is available as an output.

2. Smallest signal path. For a particular signal path, the program calculates the total area of the semiconductor chip occupied by the different compatible sizes of standard cells forming the path, and automatically selects the combination requiring the minimum area of the semiconductor chip. The total signal propagation time along the path using the selected sizes of cell is available as an output.

3. Smallest block. This is similar to 2. above but relates to the standard cells forming an entire circuit or part of a circuit and not to just a single signal path.

4. Time range path. This is a combination of 1. and 2. above in that the selection of standard cell sizes is limited to those providing a pre-determined maximum signal propagation delay time along the specified path. Within that limitation the standard cell sizes are automatically selected to require the minimum area of semiconductor chip.

5. Race path. Where two signals are to be used together in a standard cell, for example, or are otherwise used simultaneously, the propagation delays along the paths conveying the signals to that place are compared and the sizes of cell along those paths selected to provide a time delay difference within a specified range, if possible. If it is not possible to provide a time delay difference with the specified range, the nearest approach to that range will be given as an output.

6. Special requirements for multiple signal paths. Sometimes there are criteria to be met in a circuit for it to operate and such criteria must override more general desiderata of minimum signal propagation time along a particular path and minimum area of semi-conductor chip required. For example, where two paths converge at a cell and the output of the cell depends on which of its inputs receives a signal first, for a predictable effect to be obtained the signal propagation time along one path must always be less than that along the other. This restriction can be specified in addition to the other cell selection criteria. Similarly, where a signal is a pulse, the width of the pulse can determine the propgation delay tolerance along its path or of another signal. It follows that, because of the possibility of conflict between the various requirements, the final circuit may not consist of only the fastest signal paths.

7. Whole circuit optimisation. After the selection of cell sizes has been performed for the signal paths and circuit blocks separtely as described above, the entire circuit can be optimised with regard to speed, size and power consumption. When the optimum package has been selected the I/O cell types are specified to suit the input and output requirements of the circuit.

The program has five different modes, as follows:-

1. Dynamic load checking. Whenever the program selects any cell, the dynamic load checking function will automatically check that the cell response time does not exceed a preset value for that cell entered by the user.

2. Delay calculator. In this mode, the signal propagation delay time is calculated for a given path in the circuit and will normally be implemented after a particular combination of cells forming the path has been selected. For further optimisation, the size of any cell in the circuit can be changed temporarily and the effect on the propagation delay calculated. When the delay calculation mode is teminated the cell size reverts to its original value.

3. Add net load. This mode permits the user to add a load capacitance to any mode of the circuit. Two possible uses for this are:-

(a) The final integrated circuit may be required to drive a load including a capacitance, and the response time of the circuit under these conditions will need to be checked.

(b) The user can employ this mode to make sure that a certain part of his design will work as he intends before he combines it with the rest of the circuit, by introducing the effect of the output loadings of the rest of the circuit into the part that he is considering.

4. Automatic new circuit generation. After a circuit design has been completed, this mode will copy the entire design into a directory of circuits.

5. Automatic cell selection manager. In this mode the size of cells for the entire circuit are selected automatically. The user enters all the response timing requirements from input terminals to output terminals, and on the basis of this information the program selects the sizes of cells to give an optimum design for fastest response or smallest area of semi-conductor chip.

According to a second aspect of the invention there is provided a method of designing integrated circuits for special purposes by selection of standard cells and the inter-connection of the selected cells, the method including performing the following operations in a computer: entering a representation of a circuit composed of the standard cells, producing a display of the circuit using conventional symbols, storing for each standard cell its input loading or loadings, its output drive capability, its response time and the area of semiconductor chip it occupies, at least some of the standard cells having a choice of different sizes with differing loadings, drive capability and response times, checking for each cell in the circuit whether the output drive capability of the particular cell matches the input loading or loadings of the cell or cells which it is connected to drive in the circuit, and where the particular cell or one which it is driving has a choice of different sizes repeating the check for each different size, producing an output indication of which, if any, check fails, selecting in turn each combination of cells which satisfies the check and determining for the combination the aggregate signal transmission time through the circuit and the total area of semiconductor chip which the circuit would occupy, and producing an output display of the combination of cells satisfying the check with one of the following: (a) having the shortest signal transmission time; (b) requiring the

smallest total area of semiconductor chip; (c) requiring the smallest total area of semiconductor chip among those having a signal transmission time shorter than a predetermined value.

In order that the invention may be fully understood and readily carried into effect an example of it will now be described with reference to the accompanying drawings, of which:

FIGURE 1 is a diagram illustrating a hierarchichal approach to integrated circuit design;

FIGURE 2 shows a single path for a signal in an integrated circuit;

FIGURE 3 shows a divergent path for a signal;

FIGURE 4 shows a convergent path for a signal;

FIGURE 5 shows a reconvergent path for a signal;

FIGURE 6 shows another divergent path for a signal which is used as an example to explain the optimization of the design of an integrated circuit;

FIGURES 7A and 7B together form a flow diagram of a design optimization procedure;

FIGURES 8 and 9 are a flow diagram of a connection rule checking procedure; and

FIGURES 10 to 16 are a flow diagram of a cell or gate selection procedure.

With a computer-aided design work station for designing integrated circuits a user can enter via the key-board details of the standard cells which he wishes to employ in his design and the interconnections between them.

The workstation displays the design using conventional symbols so that the user can see the design as he develops it and consider the operation of the different parts of the design as they are produced. The present invention adds to the facilities provided by the workstation by automatically selecting the appropriate sizes for such standard cells as are available in diffeent sizes, taking into consideration the output drive capabilities of the cells, the loadings of the the input circuits of the cells, the response times of the cells and the delays imposed by the input capacitances of the cells. Amongst other facilities provided by the invention

are checks to ensure that where a cell has several inputs and one of those inputs must precede another input for the cell to operate satisfactorily, the delays in the circuit are, if possible, arranged so that the signal on the one input will always occur before the signal on the other input. Where such an arrangement is not possible without some additional delay component an indication may be produced and the component added either automatically by the program or in response to an input made by the user.

In addition to the operation of the circuit, the program may be arranged to take into account the area of semiconductor chip material required by the different sizes of cells. For example, a circuit design may be produced which requires the smallest total area within the limitation of a stipulated maximum circuit response time, or merely satisfying output loading limitations of the cells.

Examples of facilities which the invention can provide will now be described.

One function of the invention is to optimize cell size selection for paths in a circuit whose propagation delay specifications are critical, by selecting the "best" from available cell types. When the critical paths have been dealt with, cell sizes in the rest of the circuit are optimized. The optimization criteria are either:

a. automatic cell size selection for the least propagation delay

or

b. automatic selection of the smallest area cells to meet specified timing requirements.

Examples of the invention may also provide the following facilities:

Delay calculation along a selected path;

Electrical rules checking including load checking;

I/O cell selection for core bound or I/O bound designs;

Cell count calcualtion.

The first task is the entry of the circuit into the system. A convenient way of storing the circuit is to allocate a block to each standard cell used in the circuit listing the input and output connections to the other blocks as well as the cell type. The cell types are indicated by their functions. A possible structure for the record of a block is as follows:

GATE SIZER RECORD STRUCTURE

```
BLOCK IDENTITY
VERSION-NUMBER
INPUT-PIN:
                PIN-NAME, SIGNAL IDENTITY
                .
                .
                .
                .
                .
                .
OUTPUT-PIN:
                PIN-NAME, SIGNAL IDENTITY
                .
                .
                .
                .
                .
INTERNAL-SIGNAL
                SIGNAL IDENTITY
                FAN-IN-FROM-BLOCK:
                        BLOCK IDENTITY, BLOCK-PIN-NUMBER
                        .
                        .
                        .
                FAN-OUT-FROM-BLOCK:
                        BLOCK-IDENTITY, BLOCK-PIN-NUMBER
                        .
                        .
                        .
```

A library of standard cells is provided coded by standard cell function so that the individual cell names are not required at this stage. Details of some standard cells are given at the end of the specification. These details have been taken from "2-μm CMOS Standard Cell Data Book" published by Texas Instruments Incorporated, 1986. The invention is not limited to using cells from this library and may use cells from any set. Moreover, although the invention is of particular value with cells using CMOS technology, it can be used with cells employing other technologies.

The capacitive loading at the outputs of the circuit which are present in the final application may be added to the circuit at this time. Other input parameters which can be entered may include the maximum delay time permitted along a certain path.

From the cell library, the program uses the logic description, cell sizes, input capacitances, propagation delay, delta delays and input/output pin name. This information may be stored in any convenient format in the program so that the different items are selectivbely available.

The layout parasitic capacitances and resistances are extracted and, for long interconnects, the layout capacitance is partitioned among the nodes, thereby permitting the extraction of the interconnect resistance between the nodes. This would not be possible if all the interconnect capacitance were lumped onto one node. These parasitic values are also input to the cell size optimizer.

During operation, the program changes cell sizes to optimize timing performance. If the user requires that a particular cell size is to remain unchanged, he can specify this to the program which will ensure that no change is made.

Specific inputs required for different program modes are described later.

PROGRAM OPERATION

Hierarchical Design

Consideration of the design of the circuit in a hierarchical way is desirable for understanding and manipulating most logic designs, but it is necessary to consider the design in terms of its individual gates to perform true optimized cell selection. In Figure 1 T is the highest level circuit block of a design and B is a circuit block inside both T and A. The loading and fanout environments of the two circuit blocks B are likely to be different. True optimized cell selection cannot therefore be achieved if the circuit blocks B are treated identically. An analysis is required where all circuit blocks are broken down to the individual gate level without losing track of the circuit hierarchical structure. The following program steps maintain the structure and also result in true optimization:

1. Record the hierarchical structure of the design.
2. Break down the entire design to the primitive gate level.
3. Optimize the design.
4. Re-group the gates to recreate the structure.

Further program steps preserve the identities of the two versions of block B:

5. Modify the gate (or cell) sizes and copy block B into two new database records, B_o and B_1.
6. Change the pointers in blocks T and A to point to the new database records B_o and B_1.
7. Change the displayed graphics and text for blocks T and A to display B_o and B_1 instead of B so that the user can keep track of the changes.

Afterwards, if the user needs to change block B, he may modify either of the two versions. However, modification of a particular member of the block B family will require this member to be renamed so as to avoid confusion.

If the whole of block B is to be changed, the original block can be changed instead of changing every member.

Each time the program is run, a check on the latest updates to the individual blocks is done. When an update is detected the new versions are substituted in the next gate

optimization run and all subsequent runs.

Optimization by Cell Selection

Cell size selection is first performed on critical paths in the design whose timing specifications demand special attention. Overall optimization of the rest of the design around these paths may then be performed. For critical paths, there are two optimization criteria which can be selected.

1. Fastest Cell Selection - Cell sizes are selected to produce the lowest overall path delay irrespective of cell size.
2. Smallest Cell Selection - The delay for the path is specified and the program selects cells to meet the delay requirement using the smallest possible size cells.

There are three other ways in which a path can be handled:

1. Time range path - The cells are selected to give a signal transmission time within a range set by the user.
2. Race path - The cells are selected so that a signal transmitted along one path selected by the user always arrives before a signal transmitted along another path, thereby avoiding difficulties which might arise if two signals tending to have conflicting results arrive simultaneously.
3. Special path selection - In this case the cell selection is made by the user to suit his special requirements of it.

When further improvement of the critical path seems unlikely, overall opimization of the whole design is done. Before describing these operations in detail, an understanding of "Path Types" is desirable.

Path Types

There are four basic types of signal path in a circuit- single, divergent, convergent and reconvergent.

1. Single Path.

An example of such a path is shown in Figure 2. This is simply a selected signal path having no branches which starts at a node N1 and ends at a node N4. Such a path may include more or fewer than the three cells C1, C2, C3 shown. When using the program, the user selects the path

by entering:

a. The start node - N1.

b. The end node - N4.

c. The input signal transition carried by the path:

'R' - Rise (Low to High)

'F' - Fall (High to Low)

'B' - Both Rise and Fall

d. When required, maximum values for the propagation times from low-to-high, T_{plh}, and from high to low, T_{phl}.

During operation, the program will check that both starting and end points are nodes in the circuit design, that a path exists between these points and for the existence of any reconvergent paths by using one or more cells along the path.

2. Divergent Path.

A divergent path has one or more branches diverging from a main path in the direction of signal flow. An example of such a path is shown in Figure 3. Paths 'B' to 'C' and 'B' to 'E' are paths diverging from the main path 'A' to 'D'.

The selection of a divergent path off a main path requires the user to enter:

a. Start node on the main path at which the divergent path starts. This is node B in Figure 3.

b. End node - C or E, for example.

c. Priority of the divergent path with respect to the main path.

d. The input signal transition carried by the divergent path - as shown under c. for a Single Path.

The program checks that the start of the divergent path is on the main path and that the divergent path exists between the point on the main path and the end node. In addition, it checks that the end point is a node of the circuit, and that no reconvergent path exists.

Cell size selection will be directed by the path priorities initially entered so that high priority routes will be least affected.

3. Convergent Path.

A convergent path is one which joins the main path and has the same direction of signal flow. An example of a convergent path is shown in Figure 4 where 'G' to 'J' is a convergent path to the main path 'H' to 'K'.

To select a convergent path the user must enter:

a. The start node and the junction node of the convergent and main paths.

b. The input signal transition for both main and convergent routes (default is "both rise and fall").

c. Whether the main path or the convergent path receives an input signal first and the time difference between input signals. The program will assume signals arrive at the same time if no order is specified. If no time difference is supplied, the program defaults to 0.1ns.

d. Which signal, convergent or main path, reaches the junction point first. This may have a major effect on the junction output.

e. The minimum difference between the time of arrival of the main path and convergent path signals at the junction point. This diffference defaults to 0.1ns if no value is entered.

The program will assign sizes to the cells in both parts such that the junction point minimum time-of-arrival difference will be met. If the difference in time is greater than the required minimum, if possible the choice of cell sizes for the earlier one of the signals is made so that it will be delayed and the requirement is met. Thus faster cells are selected for the later signal and slower cells for the the earlier. When this happens an indication is sent to the user. If no combination of cell sizes can be found to satisfy the requirement, the program stops, outputs a message to the user and waits for him to change his specifications or abort the run. These safeguards have been included because of the difference of time of arrivals at signals at a junction is an important parameter which can change the path logic function and seriously affect the junction output,

particularly if the output is a pulse.

In addition to selecting cell sizes for speed, the program uses library data to check and flag a warning for the following:

a. If the junction is a synchronous gate with data and clock connected to main and convergent paths, the program will check that the specified time-of-arrival difference exceeds the set-up time for the gate.

b. If a pulse is created along a path which terminates at the data input of a synchronous gate, the program checks that the pulse length exceeds the hold-time minimum for the gate.

4. Reconvergent Paths.

A reconvergent path is one containing a branch from the main path which rejoins it at a point further along in the direction of signal flow. An example of a reconvergent path with two branches, from node 'M' to cell 'C3', is shown in Figure 5.

Selection of a reconvergent path requires the user to enter:

a. Start point - node L.

b. End point - node S.

c. The input signal transition for the path 'R', 'F', or 'B' (default).

d. Along which of the two parallel paths DR1 or DR2 (see below) the signal will reach the convergent junction cell 'C3' first. A time difference will also be required. This will default to 0.1ns if it is not specified.

The program partitions the reconvergent path into 5 parts:

1. The first single path up to the divergent junction: L - C1 - M

2. One single path (DR1) from the divergent junction to the convergent junction: M - C2 - N - C3

3. The other single path (DR2) from the divergent junction to the convergent junction: M - C5 - P - C6 - Q - C3

4. The convergent junction cell C3
5. The remaining length of path from the convergent junction to the end: C3 - R - C4 - S

The program chooses cell sizes such that the signals along the parallel paths and DR2 meet the arrival time requirements at the convergent junction cell C3. It will then optimize both paths choosing the cell sizes to give minimum delay.

General Cell Size Optimizing Technique

The program calculates delays along a path by considering the intrinsic delay for each cell along with its incremental delay per picofarad of load capacitance. This delay is calculated for each path, adding delays due to the interconnections between the cells, for both types of transitions: low-to-high and high-to-low (which are typically not equal). The program then substitutes alternative cells where possible and recalculates the total path delay. Of course cells with greater drive capabilities tend to have shorter propagation delays but offer higher load capacitances to the cells which drive them; so the overall effect of changing the size of a cell may be to lengthen or shorten the path delay. Rather than attempt all possible combinations of cell size substitutions, the program selects the statistically "most likely" choice for each cell first, and then slightly smaller and slightly larger cell selections are attempted to optimize this choice. The program stops when an optimum selection of cell sizes is found. By making such intelligent first attempts at cell size selection, unnecessary time-consuming trials of different cell sizes are avoided.

For critical paths, the algorithm in the program operates to choose the "best" cells to produce the shortest possible propagation delay. For the "rest" of the circuit, the algorithm starts with the smallest available cells and increases their sizes just until the performance specification has been reached.

A flow diagram of the cell size selection procedure is shown in Figures 10 to 16.

Fastest Cell Selection

This is the first path optimization to be considered and is normally aimed at critical timing paths in the design so that these can be fixed prior to optimization of the whole design. The aim is to select cell sizes such that the propagation delay time along the chosen path is as small as possible.

In the example of a circuit shown in Fig.6, the selected path is from node 'N1' to node 'N3'. There is, however, a branch at node 'N2' so that the input capacitance of the cell C4 must be added to that of cell C2 and the interconnection for optimum cell size computation. The input capacitance of the cell C4 depends on the size of cell chosen. The program estimates the size of the cell C4 by calculating the average load that will be called upon to drive. It finds all the cells connected to the output of the cell C4, in this case it is the cells C5 and C6, finds the input capacitance range using all possible cell sizes for C5 and C6 and takes an average value. Using this value, the program finds the minimum size of cell C4 required to meet the user's specified maximum rise/fall time for the signal at the nodes along the main path. Although this is an approximation, it provides an acceptable result in most instances.

After fixing the size for the cell C4, the program adds the appropriate input capacitance to node 'N2' and starts searching for sizes of cell along the selected path that will minimize the propagation delay.

Smallest Cell Size Selection

The purpose of this mode is to find the circuit design that occupies the smallest area of semiconductor chip material.

There are three ways of using this mode:

A/ The program selects the smallest cell sizes along the chosen path that will result in a delay less than a specified maximum.

B/ A delay time is not specified, but the program checks that the cells along the chosen path have adequate drive for the loads to which they are connected, selects the minimum sizes of cells that

will satisfy the load checker and gives the resulting delay time as output.

C/ This mode is similar to mode B, but instead of optimizing along a path, a circuit block to be optimized is indicated and the program finds the smallest sizes of cells that will satisfy the load check requirements within the block. This is especially useful for optimizing blocks in hierarchical designs.

If no suitable combination of sizes of cells can be found having the required maximum delay, the program signals the user who can then alter the timing or stop the selection.

Whole Design Optimization

Optimization of the whole design can be done iteratively with the program working initially on all cells except those in the critical paths. The procedure is shown in Figs. 7a and 7B.

The first step after schematic capture is a calculation of the total cell count N_{tot} and the total area A_{tot} occupied by all the cells in the design expressed in terms of the number of equivalent TI NA210LH two-input NAND gate cells (the smallest size) which would occupy the same area.

The program then looks at the already optimized critical paths and makes a cell count, N_{crit}, and an area calculation, A_{crit}, for these paths alone. The design core area, A_C, that enclosed by the I/O buffers selected by the user, is calculated next. The choice of minimum height or minimum width versions of the buffers may be made manually during schematic capture, but, generally, the program makes the choice automatically.

In order to calculate A_C, the program will first select an optimum silicon package, (or this package can be pre-selected by the user). The program will first calculate the 'useful area' of this package. Then by selecting the IO cells (minimum height/minimum width), which depends on the shape of the selected package, A_C can then be calculated as follows:

A_C = 'useful area - IO required - overhead.

All the internal cells in the design must fit into A_c and they will be either 'critical path' cells or 'the rest', i.e. cells of the parts of the circuit outside the critical path.

The area, A_{avail}, available for 'the rest' is clearly:

$$A_{avail} = A_c - A_{crit}$$

Also, the required area, A_{req}, for 'the rest' is:

$$A_{req} = A_{tot} - A_{crit}$$

As shown in Figs. 7A and 7B, there is sufficient area available, i.e. $A_{avail} > A_{req}$, the program searches for those cells among 'the rest' which have the highest output rise/fall times. The cell sizes of these are increased until no further improvement in rise/fall time can be made or until all the available space is used up. During this process, the program monitors the change of the power consumption. Based on the speed improvement, the area available and also the power consumption, the program will make a decision whether or not to make the selected cell bigger. At this stage the program looks at the critical paths in order to see whether the changes made in the optimization of 'the rest' have altered the performance of the critical paths: this iteration continues until a stable condition is reached.

Where the area available is insufficient, i.e. $A_{avail} < A_{req}$, the program works to adjust to the situation by first carrying out a load checking exercise. 'The rest' is examined by the load checking software which adjusts cell sizes to conform to the rules without regard to the overall area problem. An iteration is carried out via route B in Figs. 7A and 7B to make sure that these size adjustments have not affected the cell sizes in the 'critical path' portion of the circuit. After this, the I/O buffer periphery is increased by automatic selection of wider I/O buffers and spacing so as to boost the available core area. This sequence is continued until the area problem is solved.

Delay Calculation

An Interactive Timing Analyzer (ITA) permits the user to calculate the delay time along a chosen path in the circuit. Each cell in the cell library is fully characte-

rized for its minimum, maximum and typical propagation value over its rated commercial or military temperature and voltage range. The ITA is used after cell selection by one of the modes described above. For further optimization, the size of a cell in the chosen path can be temporarily changed and the effect of the change can be instantly calculated. The cell size will automatically revert to its original size when another path is chosen or when the delay calculation mode is terminated.

Electrical Rules Checking

The electrical rules checker complements the selection of cell sizes by providing a knowledge-based analysis of the complete circuit by evaluating such criteria as wrongly connected cells and checking and correcting cell-load violations such as the following:-

* Unconnected cell inputs.
* Signal inputs of a cell connected to V_{CC}.
* Cells driving themselves (exceptions: D and JK flip-flop cells).
* Unconnected output signals.
* Cell load violations - by checking that cell response time does not exceed a preset value.

A flow diagram of the rules checking procedure is shown in Figures 8 and 9.

I/O Cell Type Selection

In this mode, the total number of transistors in the design is calculated and a computation is made to determine whether the design is core bound, i.e. the minimum die size is determined by the sheet size of the core, or I/O bound, leaving an unused area inside the I/O periphery. Whether core bound or I/O bound, the program can automatically select wider or higher cells to "pull" the I/O periphery in closer to the core cells, thereby minimizing the die area.

Cell Count Calculator

In this mode, the program finds the number of each cell type used and calculates from this the equivalent number of two input NAND gates as a measure of design complexity. The total area required for the core and the routing factor is also calculated.

APPENDIX

There follow pages from "2μm CMOS Standard Cell Data Book" 1986, published by Texas Instruments Incorporated, Dallas. The pages which are in five groups relate to the following cells:

NA 210 LH - NA 260 LH	2-input positive NAND gate
NO 210 LH - NA 240 LH	2-input positive NOR gate
IV 110 LH - IV 180 LH	inverter
JKB 20 LH	JK positive-edge-triggered flip-flop
ASC 181	Arithmetic logic unit/function generator

The first three of these, NA210LH, NO210LH and IV110LH are basic elements of a digital circuit and are available in different sizes. The signal delays, chip areas, input capacitances and driving powers for the different cell sizes are given.

Cell JKB20LH is a flip-flop circuit available in one size only. Its cell area relative to NA210LH is given, as are the capacitances on its different inputs, its driving power and its response time.

The cell ADC 181 is a composite of gates and inverters of specified sizes. The cell area is given in terms of the area of cell NA210LH which is used as a standard. The capacitances on the different inputs are given as are the signal propagation delays for different states of the circuit. The output driving power of the cell is also given. The use of this cell eliminates the need to specify 62 elemental cells, but it can only be used if all its performance characteristics are acceptable. Certain adjustments can, of course, be made. For example, a buffer amplifier could be used to increase the output driving power of the circuit.

The cells described on the following pages are only a few of the 200 or so different types listed in the above data book.

electrical characteristics

PARAMETER		TEST CONDITIONS		NA210LH		NA220LH		UNIT
				TYP	MAX	TYP	MAX	
V_T Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		V
I_{CC} Supply current	SN54ASC00	V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX	V_I = V_{CC} or 0,		131		196	nA
	SN74ASC00				7.84		11.7	
C_i Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.12		0.2		pF
C_{pd} Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	0.51		1		pF

PARAMETER		TEST CONDITIONS		NA230LH		NA240LH		UNIT
				TYP	MAX	TYP	MAX	
V_T Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		V
I_{CC} Supply current	SN54ASC00	V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX	V_I = V_{CC} or 0,		254		316	nA
	SN74ASC00				15.2		19	
C_i Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.39		0.54		pF
C_{pd} Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	1.51		2.06		pF

PARAMETER		TEST CONDITIONS		NA260LH		UNIT
				TYP	MAX	
V_T Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		V
I_{CC} Supply current	SN54ASC00	V_{CC} = 4.5 V to 5.5 V, T_A = MIN to MAX	V_I = V_{CC} or 0,		433	nA
	SN74ASC00				26	
C_i Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.79		pF
C_{pd} Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	2.98		pF

CELL NAME	NETLIST HDL LABEL	FEATURES	
		TYPICAL DELAY C_L = 1 pF	RELATIVE CELL AREA TO NA210LH
NA210LH	Label: NA2nOLH A,B,Y;	2 ns	1
NA220LH		1.3 ns	1.5
NA230LH		1.1 ns	2
NA240LH		1 ns	2.5
NA260LH		0.8 ns	3.5

The SN54ASC00 is characterized for operation over the full military temperature range of −55°C to 125°C.
The SN74ASC00 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

TEXAS INSTRUMENTS
POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

electrical characteristics

PARAMETER			TEST CONDITIONS		NA210LH TYP	NA210LH MAX	NA220LH TYP	NA220LH MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current	SN54ASC00	V_{CC} = 4.5 V to 5.5 V,	V_I = V_{CC} or 0,		131		196	nA
		SN74ASC00	T_A = MIN to MAX			7.84		11.7	
C_i	Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.12		0.2		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	$t_r = t_f$ = 3 ns,	0.51		1		pF

PARAMETER			TEST CONDITIONS		NA230LH TYP	NA230LH MAX	NA240LH TYP	NA240LH MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current	SN54ASC00	V_{CC} = 4.5 V to 5.5 V,	V_I = V_{CC} or 0,		254		316	nA
		SN74ASC00	T_A = MIN to MAX			15.2		19	
C_i	Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.39		0.54		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	$t_r = t_f$ = 3 ns,	1.51		2.06		pF

PARAMETER			TEST CONDITIONS		NA260LH TYP	NA260LH MAX	UNIT
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		V
I_{CC}	Supply current	SN54ASC00	V_{CC} = 4.5 V to 5.5 V,	V_I = V_{CC} or 0,		433	nA
		SN74ASC00	T_A = MIN to MAX			26	
C_i	Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.79		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	$t_r = t_f$ = 3 ns,	2.98		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

NA210LH

PARAMETER[1]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC00			SN74ASC00			UNIT
				MIN	TYP[1]	MAX	MIN	TYP[1]	MAX	
t_{PLH}	A or B	Y	C_L = 0	0.7	0.8	1.4	0.7	0.8	1.3	ns
t_{PHL}				0.5	1	1.5	0.5	1	1.4	
t_{PLH}	A or B	Y	C_L = 1 pF	1.2	2	4	1.2	2	3.7	ns
t_{PHL}				1	2	4.2	1.1	2	3.7	
Δt_{PLH}	A or B	Y		0.5	1.2	2.7	0.5	1.2	2.5	ns/pF
Δt_{PHL}				0.5	1	2.7	0.5	1	2.3	

NA220LH

PARAMETER[1]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC00			SN74ASC00			UNIT
				MIN	TYP[1]	MAX	MIN	TYP[1]	MAX	
t_{PLH}	A or B	Y	C_L = 0	0.5	0.8	1.3	0.6	0.8	1.2	ns
t_{PHL}				0.3	0.7	1.4	0.4	0.7	1.3	
t_{PLH}	A or B	Y	C_L = 1 pF	0.8	1.3	2.4	0.9	1.3	2.2	ns
t_{PHL}				0.6	1.3	2.7	0.7	1.3	2.4	
Δt_{PLH}	A or B	Y		0.3	0.5	1.1	0.3	0.5	1	ns/pF
Δt_{PHL}				0.3	0.6	1.3	0.3	0.6	1.1	

NA230LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC00			SN74ASC00			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A or B	Y	C_L = 0	0.4	0.7	1.3	0.5	0.7	1.3	ns
t_{PHL}				0.2	0.6	1.4	0.3	0.6	1.3	
t_{PLH}	A or B	Y	C_L = 1 pF	0.7	1.1	2	0.7	1.1	1.9	ns
t_{PHL}				0.5	1	2.3	0.5	1	2	
Δt_{PLH}	A or B	Y		0.2	0.4	0.8	0.2	0.4	0.7	ns/pF
Δt_{PHL}				0.3	0.4	0.9	0.2	0.4	0.8	

NA240LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC00			SN74ASC00			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A or B	Y	C_L = 0	0.4	0.7	1.2	0.4	0.7	1.1	ns
t_{PHL}				0.1	0.5	1.2	0.2	0.5	1.1	
t_{PLH}	A or B	Y	C_L = 1 pF	0.6	1	1.8	0.6	1	1.7	ns
t_{PHL}				0.4	0.9	1.9	0.4	0.9	1.7	
Δt_{PLH}	A or B	Y		0.2	0.3	0.6	0.2	0.3	0.6	ns/pF
Δt_{PHL}				0.3	0.4	0.7	0.2	0.4	0.7	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
Δt_{PLH} = change in t_{PLH} with load capacitance
Δt_{PHL} = change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

NA260LH

PARAMETER[1]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC00			SN74ASC00			UNIT
				MIN	TYP[‡]	MAX	MIN	TYP[‡]	MAX	
t_{PLH}	A or B	Y	C_L = 0	0.4	0.6	1.2	0.5	0.6	1.1	ns
t_{PHL}				0.1	0.5	1.2	0.3	0.5	1.1	
t_{PLH}	A or B	Y	C_L = 1 pF	0.5	0.8	1.6	0.6	0.8	1.5	ns
t_{PHL}				0.3	0.7	1.7	0.4	0.7	1.5	
Δt_{PLH}	A or B	Y		0.1	0.2	0.5	0.1	0.2	0.4	ns/pF
Δt_{PHL}				0.1	0.2	0.6	0.1	0.2	0.5	

[1] Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} = propagation delay time, low to high level output
t_{PHL} = propagation delay time, high-to-low-level output
Δt_{PLH} = change in t_{PLH} with load capacitance
Δt_{PHL} = change in t_{PHL} with load capacitance
[‡] Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to Section 7

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

SN54ASC02, SN74ASC02
2-INPUT POSITIVE-NOR GATES

D2939, AUGUST 1986

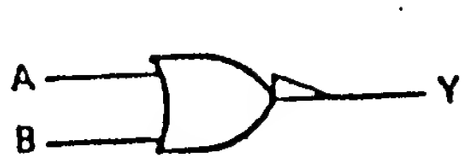
SystemCell™ 2-μm INTERNAL STANDARD CELL

- Choice of Four Performance Levels
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

positive logic equations

$$Y = \overline{A+B} = \overline{A} \cdot \overline{B}$$

logic symbol



FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

description

The SN54ASC02 and SN74ASC02 are 2-input positive-NOR gate CMOS standard-cell functions implementing the equivalent of one-fourth of the SN54LS02 or SN74LS02. The standard-cell library contains four physical implementations providing the custom IC designer a choice between four performance levels for optimizing designs. Each option is designated and called from the engineering workstation input using the following cell names to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		TYPICAL DELAY C_L = 1 pF	RELATIVE CELL AREA TO NA210LH
NO210LH	Label: NO2nOLH A,B,Y;	2.4 ns	1
NO220LH		1.5 ns	1.5
NO230LH		1.3 ns	2
NO240LH		1.1 ns	2.5

The SN54ASC02 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC02 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER		TEST CONDITIONS		NO210LH TYP	NO210LH MAX	NO220LH TYP	NO220LH MAX	UNIT
V_T Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		V
I_{CC} Supply current	SN54ASC02	V_{CC} = 4.5 V to 5.5 V,	V_I = V_{CC} or 0,		128		185	nA
	SN74ASC02	T_A = MIN to MAX			7.71		11.1	
C_i Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.11		0.24		pF
C_{pd} Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	0.33		0.52		pF

PARAMETER		TEST CONDITIONS		NO230LH TYP	NO230LH MAX	NO240LH TYP	NO240LH MAX	UNIT
V_T Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		V
I_{CC} Supply current	SN54ASC02	V_{CC} = 4.5 V to 5.5 V,	V_I = V_{CC} or 0,		237		292	nA
	SN74ASC02	T_A = MIN to MAX			14.2		17.5	
C_i Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.36		0.47		pF
C_{pd} Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	0.8		0.98		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

NO210LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC02			SN74ASC02			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A or B	Y	C_L = 0	0.6	0.8	1.6	0.6	0.8	1.5	ns
t_{PHL}				0.5	1	1.7	0.6	1	1.7	
t_{PLH}	A or B	Y	C_L = 1 pF	1.5	2.8	6.2	1.6	2.8	5.6	ns
t_{PHL}				1.1	2	4.6	1.1	2	4.1	
Δt_{PLH}	A or B	Y		0.9	2	4.6	1	2	4.2	ns/pF
Δt_{PHL}				0.5	1	2.9	0.5	1	2.5	

NO220LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC02			SN74ASC02			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A or B	Y	C_L = 0	0.6	0.8	1.3	0.6	0.8	1.2	ns
t_{PHL}				0.3	0.8	1.5	0.3	0.8	1.5	
t_{PLH}	A or B	Y	C_L = 1 pF	1	1.7	3.5	1.1	1.7	3.2	ns
t_{PHL}				0.7	1.3	2.6	0.7	1.3	2.4	
Δt_{PLH}	A or B	Y		0.4	0.9	2.3	0.5	0.9	2	ns/pF
Δt_{PHL}				0.3	0.6	1.1	0.4	0.6	1	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
Δt_{PLH} = change in t_{PLH} with load capacitance
Δt_{PHL} = change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (continued)

NO230LH

PARAMETER[1]	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC02			SN74ASC02			UNIT
				MIN	TYP[‡]	MAX	MIN	TYP[‡]	MAX	
t_{PLH}	A or B	Y	C_L = 0	0.5	0.8	1.4	0.5	0.8	1.2	ns
t_{PHL}				0.3	0.7	1.6	0.3	0.7	1.5	
t_{PLH}	A or B	Y	C_L = 1 pF	0.9	1.4	2.9	0.9	1.4	2.6	ns
t_{PHL}				0.6	1.2	2.4	0.6	1.2	2.2	
Δt_{PLH}	A or B	Y		0.3	0.6	1.5	0.3	0.6	1.4	ns/pF
Δt_{PHL}				0.2	0.5	0.9	0.3	0.5	0.8	

NO240LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC02			SN74ASC02			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A or B	Y	C_L = 0	0.5	0.7	1.3	0.5	0.7	1.2	ns
t_{PHL}				0.2	0.6	1.4	0.2	0.6	1.3	
t_{PLH}	A or B	Y	C_L = 1 pF	0.7	1.2	2.4	0.8	1.2	2.2	ns
t_{PHL}				0.5	1	2.1	0.5	1	1.9	
Δt_{PLH}	A or B	Y		0.2	0.5	1.2	0.3	0.5	1.1	ns/pF
Δt_{PHL}				0.2	0.4	0.7	0.2	0.4	0.6	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
Δt_{PLH} = change in t_{PLH} with load capacitance
Δt_{PHL} = change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to Section 7.

SN54ASC04, SN74ASC04
INVERTERS

D2939, AUGUST 1986

SystemCell™ 2-μm INTERNAL STANDARD CELL

- Choice of Seven Performance Levels
- Specified for Operation Over V_{CC} Range of 4.5 V to 5.5 V
- Functional Operation Over V_{CC} Range of 2 V to 6 V
- Dependable Texas Instruments Quality and Reliability

positive logic equation

$$Y = \overline{A}$$

logic symbol

FUNCTION TABLE

INPUT A	OUTPUT Y
H	L
L	H

description

The SN54ASC04 and SN74ASC04 are CMOS inverter standard cells implementing the equivalent of one-sixth of a SN54LS04 or SN74LS04. The standard-cell library contains seven physical implementations providing the custom IC designer a choice of seven performance levels for optimizing designs. Each of the options are designated and called from the engineering workstation input using the following cell names to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		TYPICAL DELAY C_L = 1 pF	RELATIVE CELL AREA TO NA210LH
IV110LH	Label: IV1n0LH A,Y;	1.7 ns	0.75
IV120LH		1.1 ns	1
IV130LH		0.9 ns	1.25
IV140LH		0.8 ns	1.5
IV160LH		0.7 ns	2
IV180LH		0.6 ns	2.5
IV101LH	Label: IV101LH A,Y;	2.3 ns	4.5

The SN54ASC04 is characterized for operation over the full military temperature range of −55°C to 125°C.
The SN74ASC04 is characterized for operation from −40°C to 85°C.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER		TEST CONDITIONS		IV110LH TYP	IV110LH MAX	IV120LH TYP	IV120LH MAX	UNIT
V_T Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		V
I_{CC} Supply current	SN54ASC04	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX			105		131	nA
	SN74ASC04				6.32		7.85	
C_i Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.12		0.24		pF
C_{pd} Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	0.44		0.8		pF

PARAMETER		TEST CONDITIONS		IV130LH TYP	IV130LH MAX	IV140LH TYP	IV140LH MAX	UNIT
V_T Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		V
I_{CC} Supply current	SN54ASC04	V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX			163		190	nA
	SN74ASC04				9.76		11.4	
C_i Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.4		0.49		pF
C_{pd} Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	1.29		1.61		pF

PARAMETER			TEST CONDITIONS		IV160LH		IV180LH		UNIT
					TYP	MAX	TYP	MAX	
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current	SN54ASC04	V_{CC} = 4.5 V to 5.5 V,	V_I = V_{CC} or 0,		247		306	nA
		SN74ASC04	T_A = MIN to MAX			14.8		18.4	
C_i	Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.74		1		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	$t_r = t_f$ = 3 ns,	2.39		3.16		pF

PARAMETER			TEST CONDITIONS		IV101LH		UNIT
					TYP	MAX	
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		V
I_{CC}	Supply current	SN54ASC04	V_{CC} = 4.5 V to 5.5 V,	V_I = V_{CC} or 0,		553	nA
		SN74ASC04	T_A = MIN to MAX			33.2	
C_i	Input capacitance		V_{CC} = 5 V,	T_A = 25°C	0.13		pF
C_{pd}	Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C	$t_r = t_f$ = 3 ns,	7.22		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

IV110LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC04			SN74ASC04			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	C_L = 0	0.6	0.8	1.1	0.6	0.8	1.1	ns
t_{PHL}				0.4	0.9	1.4	0.5	0.9	1.4	
t_{PLH}	A	Y	C_L = 1 pF	1.1	1.8	3.4	1.2	1.8	3.2	ns
t_{PHL}				0.9	1.6	3.2	1	1.6	2.9	
Δt_{PLH}	A	Y		0.5	1	2.3	0.5	1	2.1	ns/pF
Δt_{PHL}				0.5	0.8	1.8	0.5	0.8	1.6	

IV120LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC04			SN74ASC04			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	C_L = 0	0.4	0.6	1.1	0.4	0.6	1	ns
t_{PHL}				0.2	0.6	1.2	0.2	0.6	1.1	
t_{PLH}	A	Y	C_L = 1 pF	0.8	1.2	2.1	0.8	1.2	2	ns
t_{PHL}				0.5	1	2.1	0.6	1	2	
Δt_{PLH}	A	Y		0.3	0.5	1.1	0.3	0.5	1	ns/pF
Δt_{PHL}				0.3	0.5	0.9	0.3	0.5	0.9	

IV130LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC04			SN74ASC04			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	C_L = 0	0.4	0.6	1.1	0.4	0.6	1	ns
t_{PHL}				0.03	0.3	0.9	0 08	0.3	0.8	
t_{PLH}	A	Y	C_L = 1 pF	0.7	1	1.8	0.7	1	1.7	ns
t_{PHL}				0.2	0.7	1.5	0.3	0.7	1.4	
Δt_{PLH}	A	Y		0.2	0.4	0.8	0.2	0.4	0.7	ns/pF
Δt_{PHL}				0.2	0.4	0.7	0.2	0.4	0.6	

IV140LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC04			SN74ASC04			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	C_L = 0	0.4	0.5	0.9	0.4	0.5	0.9	ns
t_{PHL}				0.1	0.4	0.9	0.1	0.4	0.8	
t_{PLH}	A	Y	C_L = 1 pF	0.6	0.9	1.5	0.6	0.9	1.4	ns
t_{PHL}				0.3	0.7	1.5	0.3	0.7	1.4	
Δt_{PLH}	A	Y		0.2	0.3	0.6	0.2	0.3	0.6	ns/pF
Δt_{PHL}				0.2	0.3	0.6	0.2	0.3	0.6	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low level output
Δt_{PLH} = change in t_{PLH} with load capacitance
Δt_{PHL} = change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

IV160LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC04			SN74ASC04			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	C_L = 0	0.3	0.5	0.8	0.3	0.5	0.8	ns
t_{PHL}				0.09	0.3	0.8	0.1	0.3	0.8	
t_{PLH}	A	Y	C_L = 1 pF	0.5	0.7	1.3	0.5	0.7	1.2	ns
t_{PHL}				0.2	0.6	1.3	0.3	0.6	1.2	
Δt_{PLH}	A	Y		0.1	0.2	0.5	0.1	0.2	0.5	ns/pF
Δt_{PHL}				0.1	0.2	0.5	0.1	0.2	0.5	

IV180LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC04			SN74ASC04			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	C_L = 0	0.3	0.4	0.8	0.3	0.4	0.7	ns
t_{PHL}				0.08	0.3	0.8	0.1	0.3	0.7	
t_{PLH}	A	Y	C_L = 1 pF	0.4	0.6	1.1	0.4	0.6	1.1	ns
t_{PHL}				0.2	0.5	1.1	0.2	0.5	1	
Δt_{PLH}	A	Y		0.1	0.2	0.4	0.1	0.2	0.4	ns/pF
Δt_{PHL}				0.1	0.2	0.4	0.1	0.2	0.4	

IV101LH

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC04			SN74ASC04			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	A	Y	C_L = 0	1.3	2.3	5	1.3	2.3	4.5	ns
t_{PHL}				1	2	4.6	1	2	4.1	
t_{PLH}	A	Y	C_L = 1 pF	1.3	2.4	5.2	1.4	2.4	4.7	ns
t_{PHL}				1	2.1	4.9	1.1	2.1	4.4	
Δt_{PLH}	A	Y		60	120	230	60	120	200	ps/pF
Δt_{PHL}				30	110	290	50	110	280	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
Δt_{PLH} = change in t_{PLH} with load capacitance
Δt_{PHL} = change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

DESIGN CONSIDERATIONS

Refer to Section 7.

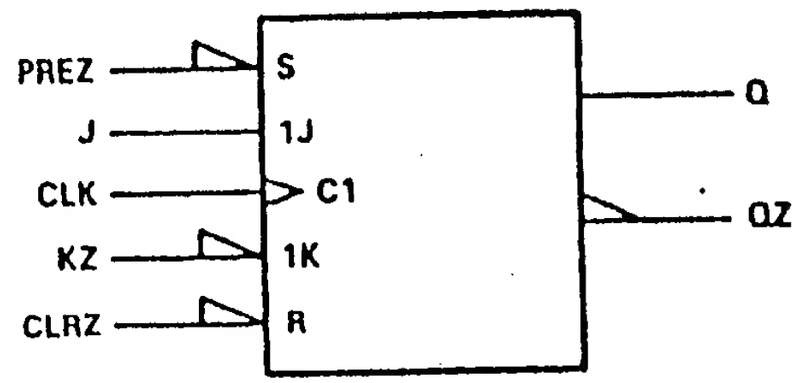
SN54ASC109, SN74ASC109
J-$\overline{K}$ POSITIVE-EDGE-TRIGGERED FLIP-FLOPS

D2939, AUGUST 1986

SystemCell™ 2-μm HARDWIRED MACRO CELL

- Provides Complementary Q and QZ Outputs
- Positive-Edge Triggered with J and KZ Data Inputs
- CLRZ and PREZ Inputs Provide Asynchronous Initialization
- J and KZ Inputs Simplify Implementation of Toggle Flip-Flops

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

description

The SN54ASC109 and SN74ASC109 are dedicated, hardwired, standard-cell macros implementing positive-edge-triggered flip-flops. A low level at the PREZ or CLRZ input controls the state of the outputs regardless of the levels of the other inputs. When PREZ AND CLRZ are inactive (high), data at the J and KZ inputs meeting the setup time requirements are transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock transition. Following the hold time interval, data at the J and KZ inputs may be changed without affecting the levels at the outputs. These versatile flip-flops can perform as D-type flip-flops if J and KZ are tied together. The JK2OLH flip-flop implements the function and sequential operation identical to one-half of the 'LS109, 'S109, or 'F109 packaged flip-flops. The cell is designated and called from the engineering workstation input using the following cell name to develop labels for the design netlist:

CELL NAME	NETLIST HDL LABEL	FEATURES	
		MAXIMUM CLOCK FREQUENCY	RELATIVE CELL AREA TO NA210LH
JKB20LH	Label: JKB20LH CLRZ,PREZ,J,KZ,CLK,Q,QZ;	44.2 MHz	10

The SN54ASC109 is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74ASC109 is characterized for operation from −40°C to 85°C.

FUNCTION TABLE

INPUTS					OUTPUTS	
PREZ	CLRZ	CLK	J	KZ	Q	QZ
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H‡	H‡
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q_0	$\overline{Q}_0$
H	H	↑	H	H	H	L
H	H	L	X	X	Q_0	$\overline{Q}_0$

‡ This configuration is nonstable; that is, it will not persist when PREZ or CLRZ return to their inactive (high) level.

absolute maximum ratings and recommended operating conditions

See Table 1 in Section 2.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

		MIN	MAX	UNIT
f_{max} Clock frequency		0	44.2	MHz
t_w Pulse duration	CLRZ low	9		ns
	PREZ low	9		
	CK High	11.4		
	CK low	11.4		
t_{su} Setup time	CLRZ inactive	1.8		ns
	PREZ inactive	−0.4		
t_h Hold time	J or KZ low	9		ns
	CLRZ low	3		
	PREZ low	9.6		
	J or KZ high or low	0		

electrical characteristics

PARAMETER		TEST CONDITIONS	SN54ASC019		SN74ASC019		UNIT
			TYP	MAX	TYP	MAX	
V_T Input threshold voltage		V_{CC} = 5 V, T_A = 25°C	2.2		2.2		V
I_{CC} Supply current		V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN to MAX		1181		70.9	nA
C_i Input capacitance	PREZ or CLRZ	V_{CC} = 5 V, T_A = 25°C	0.25		0.25		pF
	J		0.12		0.12		
	KZ		0.13		0.13		
	CLK		0.13		0.13		
C_{pd} Equivalent power dissipation capacitance		V_{CC} = 5 V, T_A = 25°C, $t_r = t_f$ = 3 ns,	4.81		4.81		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC109			SN74ASC109			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{PLH}	CLK	Q,QZ	C_L = 0	1.8	5	13.5	2	5	11.9	ns
t_{PHL}				1.9	4.5	12.2	2.1	4.5	10.9	
t_{PLH}	PREZ,CLRZ	Q,QZ		2	4.2	11	2.2	4.2	9.8	ns
t_{PHL}				1.1	2.2	5.2	1.2	2.2	4.7	
t_{PLH}	CLK	Q,QZ	C_L = 1 pF	2.1	5.5	14.6	2.3	5.5	13	ns
t_{PHL}				2.1	4.9	13.1	2.2	4.9	11.7	
t_{PLH}	PREZ,CLRZ	Q,QZ		2.3	4.7	12.2	2.5	4.7	10.9	ns
t_{PHL}				1.3	2.6	6.4	1.4	2.6	5.8	
Δt_{PLH}	Any	Q,QZ		0.2	0.5	1.3	0.2	0.5	1.2	ns/pF
Δt_{PHL}				0.1	0.4	1.2	0.1	0.4	1.1	

† Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f$ = 3 ns (10% and 90%).
t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output
Δt_{PLH} = change in t_{PLH} with load capacitance
Δt_{PHL} = change in t_{PHL} with load capacitance
‡ Typical values are at V_{CC} = 5 V, T_A = 25°C.

D2939, AUGUST 1986

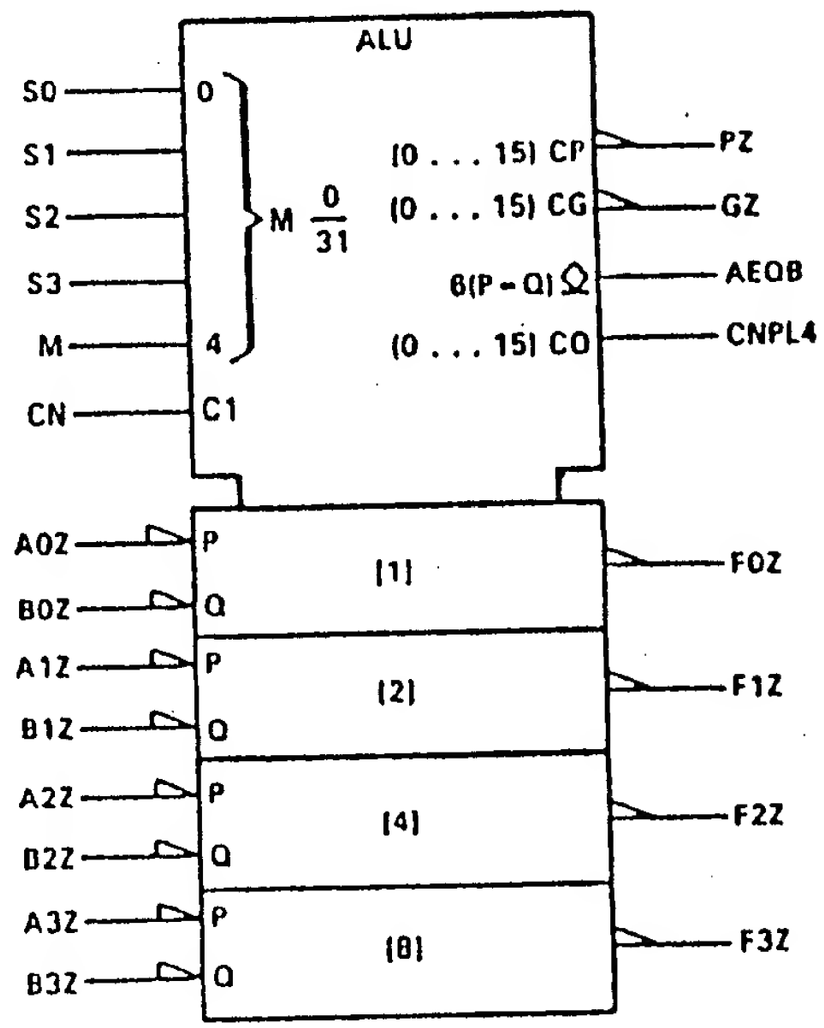
SystemCell™ 2-μm SOFTWARE MACRO CELL

- Performs Full 16-Function Arithmetic or Boolean Combinations of Two Variables
- Arithmetic Operating Modes:
  - Addition
  - Subtraction
  - Shift Operand A One Position
  - Magnitude Comparison
  - Plus Twelve Other Arithmetic Operations
- Logic Function Modes:
  - Exclusive-OR
  - Comparator
  - AND, NAND, OR, NOR
  - Plus Ten Other Logic Operations

description

The SN54ASC181 and SN74ASC181 are standard-cell software macro 4-bit arithmetic logic units. The 'ASC181 implements a function table identical with that performed by packaged 'LS181, 'S181, and 'F181 arithmetic logic units/function generators.

logic symbol†



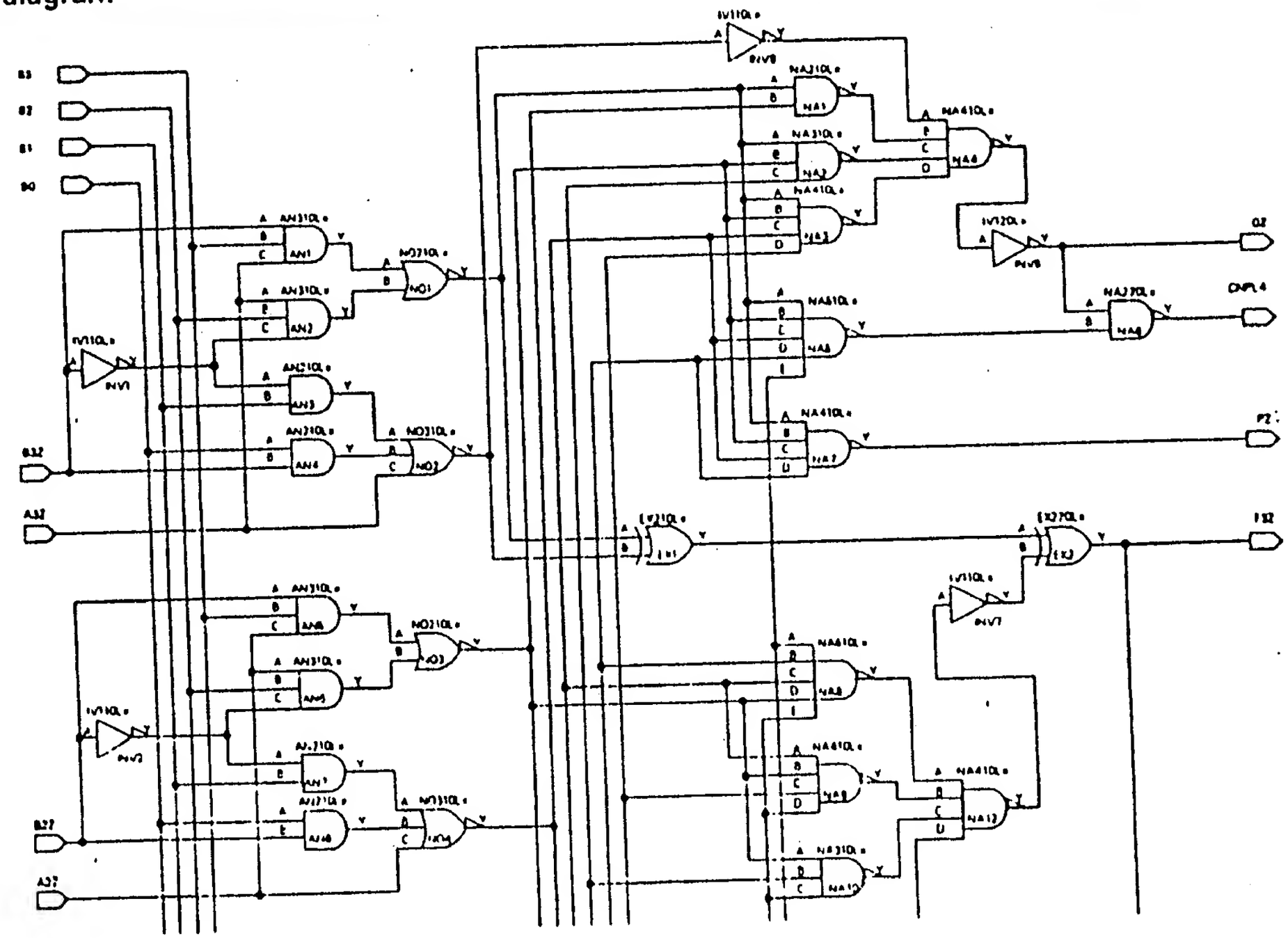
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

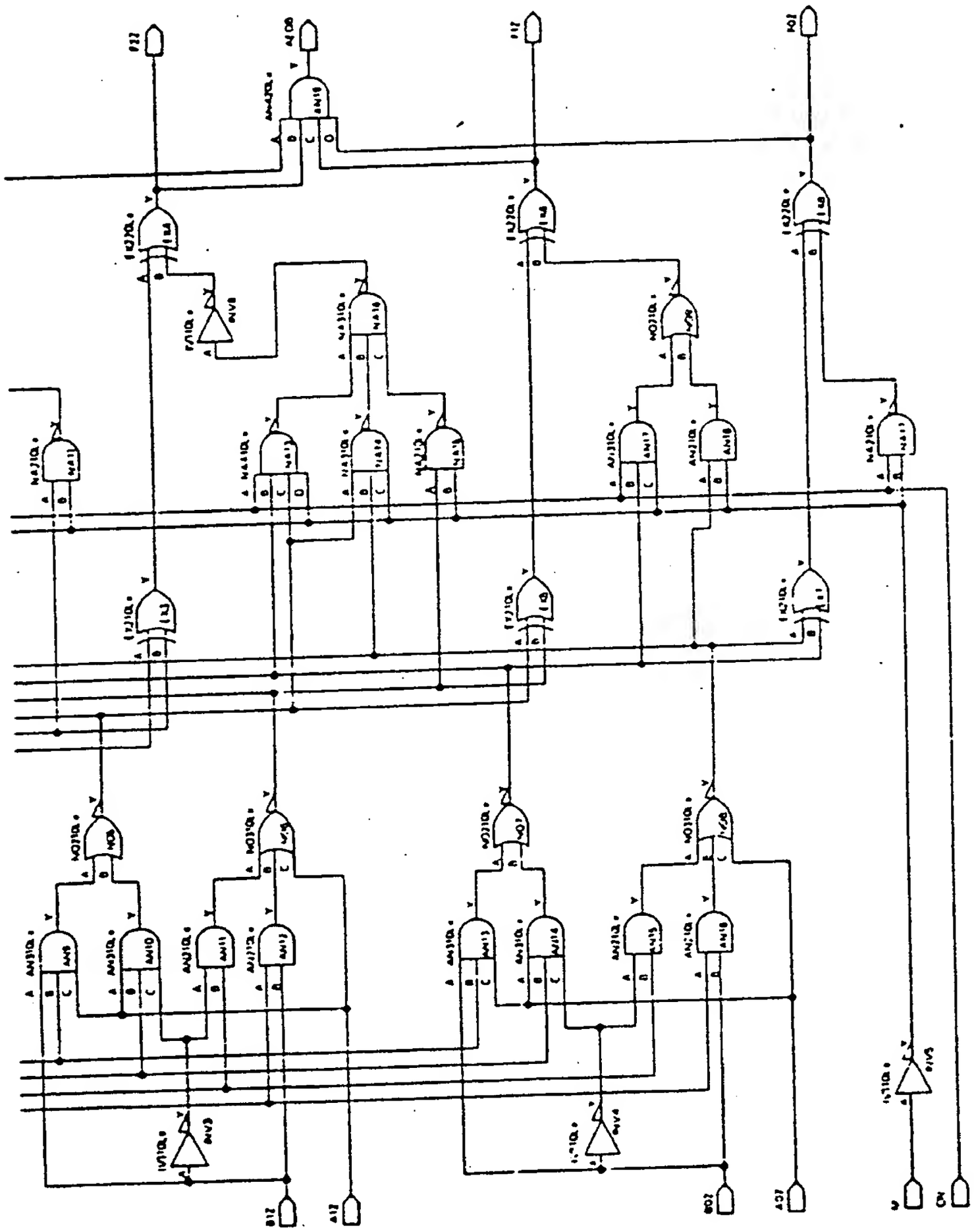
The 'ASC181 performs 16 arithmetic or Boolean operations on two 4-bit binary words as shown in Tables 1 and 2. Choice between the two operating modes is established by the mode control, M, and selection of one-of-sixteen operations is accomplished at the select inputs S3, S2, S1, and S0. The 'ASC181 is implemented with the standard cell functions indicated. The HDL netlist label for this software macro is shown on the last line of the following table:

CELL NAME	RELATIVE CELL AREA TO NA210LH	NO. USED	TOTAL RELATIVE CELL AREA	TOTAL C_{pd}[1] (pF)	MAXIMUM I_{CC} (nA)	
					SN54ASC'	SN74ASC'
AN210LH	1.5	9	13.5	8.1	1746	104.4
AN310LH	1.75	9	15.75	9.54	1989	119.7
AN420LH	2.25	1	2.25	1.72	286	17.2
EX210LH	2	4	8	4.48	892	53.6
EX220LH	2.25	4	9	6	1032	62
IV110LH	0.75	8	6	3.52	840	50.56
IV120LH	1	1	1	0.8	131	7.85
NA210LH	1	4	5	2.55	655	39.2
NA220LH	1.5	1	1.5	1	196	11.7
NA310LH	1.25	4	5	2	652	39.12
NA410LH	1.5	6	9	3	1122	67.2
NA510LH	1.75	2	3.5	1.04	426	25.6
NO210LH	1	5	5	1.65	640	38.55
NO310LH	1.25	4	5	1.28	624	37.32
TOTALS		62	89.5	46.68	11231	675
Label: S181LH A3Z,A2Z,A1Z,A0Z,B3Z,B2Z,B1Z,B0Z,CN,M,S3,S2,S1,S0,F3Z,F2Z, F1Z,F0Z,AEQB,GZ,PZ,CNPL4;						

[1]The equivalent power dissipation capacitance does not include interconnect capacitance.

logic diagram





signal designations

The polarity indicators (open arrowheads) in both Figures 1 and 2 indicate that the associated input or output is active-low with respect to the function shown inside the symbol, and the symbols are the same in both figures. The signal designations in Figure 1 agree with the indicated internal functions based on active-low data and are for use with the logic functions and arithmetic operations shown in Table 1. The signal designations used in Figure 2 accommodate the logic functions and arithmetic operations for the active-high data given in Table 2.

FIGURE 1

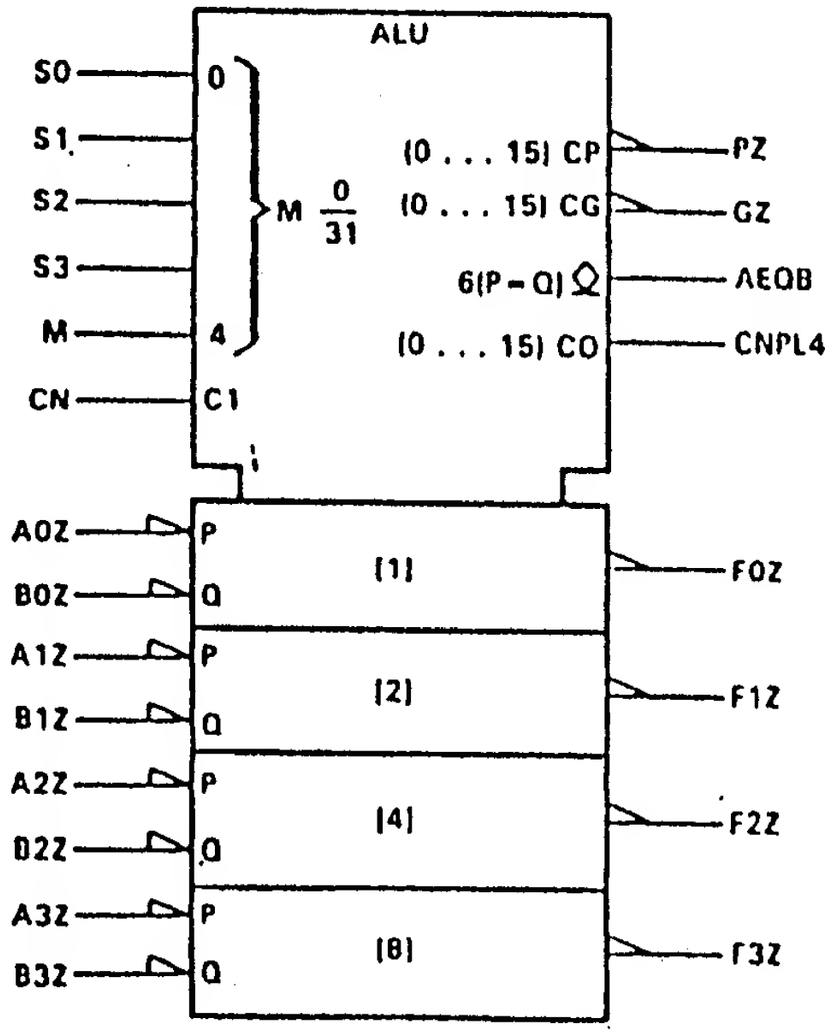


FIGURE 2

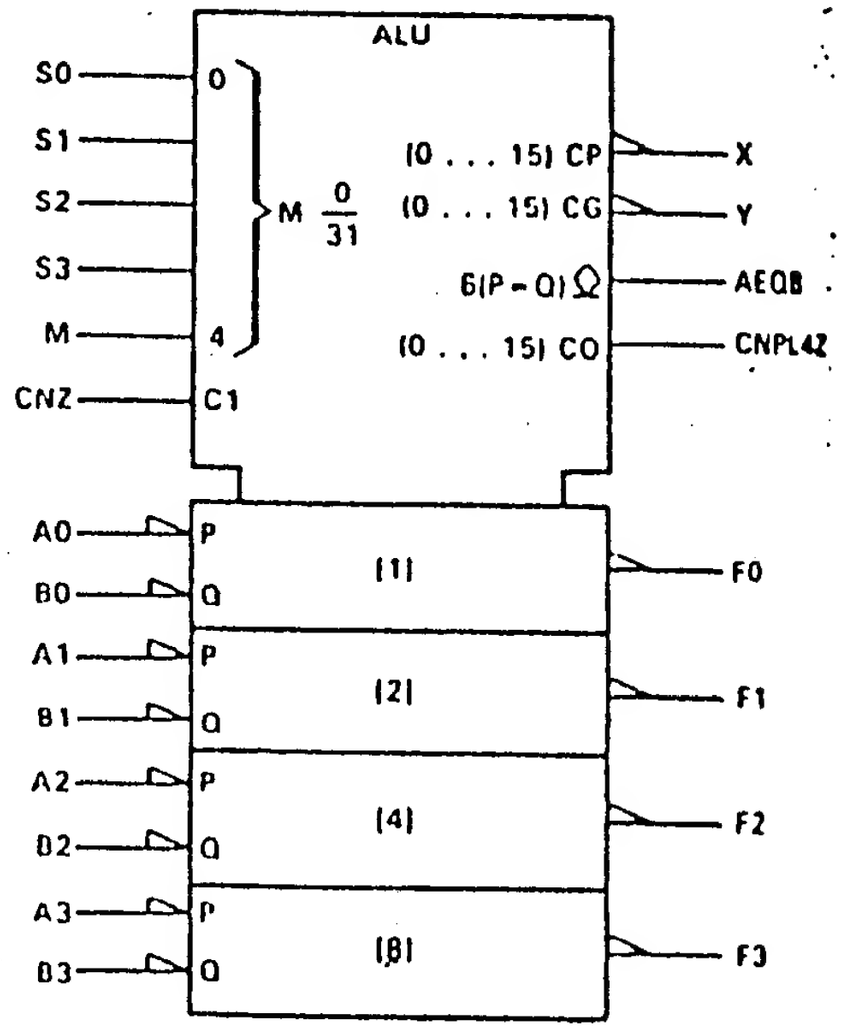


TABLE 1

SELECTION				ACTIVE-LOW DATA		
				M = H	M = L; ARITHMETIC OPERATIONS	
S3	S2	S1	S0	LOGIC FUNCTIONS	CN = L (no carry)	CN = H (with carry)
L	L	L	L	$F = \overline{A}$	F = A MINUS 1	F = A
L	L	L	H	$F = \overline{AB}$	F = AB MINUS 1	F = AB
L	L	H	L	$F = \overline{A} + B$	$F = A\overline{B}$ MINUS 1	$F = A\overline{B}$
L	L	H	H	F = 1	F = MINUS 1 (2's COMP)	F = ZERO
L	H	L	L	$F = \overline{A + B}$	F = A PLUS (A + $\overline{B}$)	F = A PLUS (A + $\overline{B}$) PLUS 1
L	H	L	H	$F = \overline{B}$	F = AB PLUS (A + $\overline{B}$)	F = AB PLUS (A + $\overline{B}$) PLUS 1
L	H	H	L	$F = \overline{A \oplus B}$	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	$F = A + \overline{B}$	$F = A + \overline{B}$	F = (A + $\overline{B}$) PLUS 1
H	L	L	L	$F = \overline{A}B$	F = A PLUS (A + B)	F = A PLUS (A + B) PLUS 1
H	L	L	H	$F = A \oplus B$	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	$F = A\overline{B}$ PLUS (A + B)	$F = A\overline{B}$ PLUS (A + B) PLUS 1
H	L	H	H	F = A + B	F = (A + B)	F = (A + B) PLUS 1
H	H	L	L	F = 0	F = A PLUS A*	F = A PLUS A PLUS 1
H	H	L	H	$F = A\overline{B}$	F = AB PLUS A	F = AB PLUS A PLUS 1
H	H	H	L	F = AB	$F = A\overline{B}$ PLUS A	$F = A\overline{B}$ PLUS A PLUS 1
H	H	H	H	F = A	F = A	F = A PLUS 1

*Each bit is shifted to the next more significant position.

TABLE 2

SELECTION				ACTIVE-HIGH DATA		
				M = H	M = L; ARITHMETIC OPERATIONS	
S3	S2	S1	S0	LOGIC FUNCTIONS	CNZ = H (no carry)	CNZ = L (with carry)
L	L	L	L	$F = \overline{A}$	F = A	F = A PLUS 1
L	L	L	H	$F = \overline{A + B}$	F = A + B	F = (A + B) PLUS 1
L	L	H	L	$F = \overline{A}B$	$F = A + \overline{B}$	$F = (A + \overline{B})$ PLUS 1
L	L	H	H	F = 0	F = MINUS 1 (2's COMP)	F = ZERO
L	H	L	L	$F = \overline{AB}$	$F = A$ PLUS $A\overline{B}$	$F = A$ PLUS $A\overline{B}$ PLUS 1
L	H	L	H	$F = \overline{B}$	$F = (A + B)$ PLUS $A\overline{B}$	$F = (A + B)$ PLUS $A\overline{B}$ PLUS 1
L	H	H	L	$F = A \oplus B$	F = A MINUS B MINUS 1	F = A MINUS B
L	H	H	H	$F = A\overline{B}$	$F = A\overline{B}$ MINUS 1	$F = A\overline{B}$
H	L	L	L	$F = \overline{A} + B$	F = A PLUS AB	F = A PLUS AB PLUS 1
H	L	L	H	$F = \overline{A \oplus B}$	F = A PLUS B	F = A PLUS B PLUS 1
H	L	H	L	F = B	$F = (A + \overline{B})$ PLUS AB	$F = (A + \overline{B})$ PLUS AB PLUS 1
H	L	H	H	F = AB	F = AB MINUS 1	F = AB
H	H	L	L	F = 1	F = A PLUS A*	F = A PLUS A PLUS 1
H	H	L	H	$F = A + \overline{B}$	F = (A + B) PLUS A	A = (A + B) PLUS A PLUS 1
H	H	H	L	F = A + B	$F = (A + \overline{B})$ PLUS A	$F = (A + \overline{B})$ PLUS A PLUS 1
H	H	H	H	F = A	F = A MINUS 1	F = A

*Each bit is shifted to the next more significant position.

maximum ratings and recommended operating conditions

See Table 1 in Section 2.

electrical characteristics

PARAMETER			TEST CONDITIONS		SN54ASC181		SN74ASC181		UNIT
					TYP	MAX	TYP	MAX	
V_T	Input threshold voltage		V_{CC} = 5 V,	T_A = 25°C	2.2		2.2		V
I_{CC}	Supply current		V_{CC} = 4.5 V to 5.5 V, V_I = V_{CC} or 0, T_A = MIN or MAX			11231		675	nA
C_i	Input capacitance	An, Bn	V_{CC} = 5 V,	T_A = 25°C	0.36		0.36		pF
		Sn			0.5		0.5		
		M			0.12		0.12		
		CN			0.6		0.6		
C_{pd}	Equivalent power dissipation capacitance[1]		V_{CC} = 5 V, T_A = 25°C	t_r = t_f = 3 ns,	46.68		46.68		pF

[1] The equivalent power dissipation capacitance does not include interconnect capacitance.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note 1)

PARAMETER†	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	SN54ASC181			SN74ASC181			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
t_{pd}	CN	CNPL4			3	8		3	7	ns
t_{pd}	AnZ or BnZ	CNPL4	SUM mode		7	15		7	14	ns
t_{pd}			DIFF mode							
t_{pd}	CN	Fn	SUM or DIFF		7	14.4		7	12.9	ns
t_{pd}	AnZ or BnZ	GZ	SUM mode		6	13.8		6	12.8	ns
t_{pd}			DIFF mode							
t_{pd}	AnZ or BnZ	PZ	SUM mode		7	15.4		7	14.1	ns
t_{pd}			DIFF mode							
t_{pd}	AiZ or BiZ	FiZ	SUM mode		12	28		12	25.6	ns
t_{pd}			DIFF mode							
t_{pd}	AnZ or BnZ	AEQB	DIFF mode		13	28.4		13	25.5	ns
Δt_{pd}	Any	CNPL4		0.3	0.6	1.3	0.3	0.6	1.1	ns/pF
Δt_{pd}	AnZ or BnZ	GZ		0.3	0.5	1.1	0.3	0.5	1	ns/pF
Δt_{pd}	AnZ or BnZ	PZ		0.5	1.6	4.8	0.5	1.6	4.1	ns/pF
Δt_{pd}	Any	FiZ		0.3	0.5	1.9	0.3	0.5	1.7	ns/pF
Δt_{pd}	Any	AEQB		0.1	0.5	1.3	0.1	0.5	1.2	ns/pF

†Propagation delay times are measured from the 44% point of V_I to the 44% point of V_O with $t_r = t_f = 3$ ns (10% and 90%).
t_{pd} = propagation delay time, low-to-high or high-to-low-level output
Δt_{pd} = change in t_{pd} with load capacitance
‡Typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.
NOTE 1: These switching characteristics are simulations of the software macro cell using interconnect capacitance values for an array design having 2,000 gates. Post-layout simulation uses actual interconnect capacitance values.

All inputs to this cell must be accounted for in the netlist used to generate the next level of an ASIC design. A tie-off cell is offered specifically for managing unused inputs.

The HDL for this soft macro is included as a part of the library supplied for supported engineering workstations so that a single label can be developed to apply the macro as needed. The following printout of the HDL block definition is furnished for reference.

CLAIMS:

1. A method of manufacturing an integrated circuit including entering into a computer in response to a functional specification inputs representing a circuit design containing only selected items from a set of standard units, which design performs the logical functions of the specification, causing the components to derive from a memory recording details of the standard units of the set the response times, input loadings and output drive capabilities of different sizes of the standard units used in the circuit design, causing the computer to determine from the circuit design and the input loadings and the output drive capabilities of standard units when interconnected in accordance with the circuit design selected sizes for the standard units to match in each case the output drive capability of a unit to the total input loading of the unit or units which the particular unit is required to drive, causing the computer to produce an output display of the selected sizes of the standard units used in circuit design, producing from the display layout diagrams of an integrated circuit of the ciruit design using the selected sizes of standard units and using the layout diagrams to fabricate the integrated circuit.

2. A method according to claim 1 in which the details of the standard units recorded in the memory include the propagation delays for signals through the units, the memory also records indications that the propagation delays of certain signal paths through the circuit are critical and the computer is caused to check that the propagation delay specifications for the certain signal paths are met.

3. A method according to claim 2, wherein the sizes of the standard units are selected to give the smallest propagation delay time.

4. A method according to claim 2, wherein the sizes of the standard units are selected to be the smallest for which the certain signal paths through the circuit meet the propagation delay specifications.

5. A method according to claim 2, 3 or 4, wherein the computer is also programmed to calculate the signal propagation delay along a selected signal path for given sizes of standard units.

6. A method according to any preceding claim wherein the input loadings of the final integrated circuit are checked against specified values.

7. A method according to any preceding claim wherein the output capabilities of the final integrated circuit are checked against specified values.

8. A method according to claim 2, wherein the computer is programmed to calculate the total signal delays along a selected signal path for different compatible sizes of the standard units making up the selected signal path, to select the unit sizes giving the fastest signal propagation along the selected path, and to calculate and produce as an output the area of semiconductor material required to construct the signal path using the selected unit sizes.

9. A method according to claim 2 in which two signals are propagated through the circuit at the same time for simultaneous use in the same standard unit or otherwise, and the computer is programmed to check that the difference between the propagation delays along the respective paths of the two signals lies within a specified range.

10. A method according to any preceding claim wherein on completion of the selection of sizes of the standard units making up a circuit design a representation of the entire design is stored in the memory of the computer in a directory of circuits.

11. A method of designing integrated circuits for special purposes by selection of standard units and the interconnection of the selected units, the method including performing the following operations in a computer: entering a representation of a circuit composed of the standard units, producing a display of the circuit using conventional symbols, storing for each standard unit its input loading or loadings, its output drive capability, its response time and the area of semiconductor chip it occupies, at least some of the standard units having a choice of different sizes with differing loadings, drive capability and response times, checking for each unit in the circuit whether the output drive capability of the particular unit matches the input loading or loadings of the unit or units which it is connected to drive in the circuit, and where the particular unit or one which it is driving has a choice of different sizes repeating the check for each different size, producing an output indication of which, if any, check fails, selecting in turn each combination of units which satisfies the check and determining for the combination the aggregate signal transmission time through the circuit and the total area of semiconductor chip which the circuit would occupy, and producing an output display of the combination of units satisfying the check with one of the following: (a) having the shortest signal transmission time; (b) requiring the smallest total area of semiconductor chip; (c) requiring the smallest total area of semiconductor chip among those having a signal transmission time shorter than a predetermined value.

12. A method of manufacturing an integrated circuit substantially as described herein and as illustrated by the accompanying drawings.

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